EXHIBIT 12

Filed: October 11, 2022

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

MICRON TECHNOLOGY, INC.; MICRON SEMICONDUCTOR PRODUCTS, INC.; and MICRON TECHNOLOGY TEXAS LLC,
Petitioner,

v.

NETLIST, INC.,
Patent Owner.

Case IPR2022-00236
Patent 9,824,035 B2

PATENT OWNER'S RESPONSE
UNDER 37 C.F.R. § 42.120

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I. INTRODUCTION

Netlist, Inc. ("Patent Owner") submits this Response to the Petition ("Petition" or "Pet.") of Micron Technology, Inc., Micron Semiconductor Products, Inc., and Micron Technology Texas LLC ("Petitioners") seeking *inter partes* review ("IPR") of U.S. Patent No. 9,824,035 ("the '035 Patent").

Petitioners have wholly failed to meet their burden of establishing that the '035 Patent's claims are rendered obvious by the proposed combinations, in several instances failing even to **allege** that each claim limitation is present in or rendered obvious by any reference. To start, in all three Grounds, Petitioners' reliance on the Tokuhiro reference to satisfy the "*obtain timing information*" limitation is wholly deficient, as Tokuhiro merely incorporates a prior art method of write leveling that the '035 Patent acknowledges is insufficient to ensure proper timing of the control and data signals received and transmitted by memory modules.

Additionally, in each Ground, Petitioners fail to offer proof that the references disclose or render obvious certain limitation of the challenged claims. In Ground 1, for example, Petitioners fail to allege that Osanai discloses "*logic . . . further configured to control timing of the respective data and strobe signals on the data paths in accordance with the timing information*." In Ground 2, Petitioners do not identify any "*module control device*" in Takefman that is capable of sending "*module control signals*" to memory devices. To fill the gaps in their proof,

Petitioners improperly rely on conclusory and unsupported expert testimony, which is insufficient to prove invalidity. Petitioners' "analysis" for Ground 3 totals less than a page and a half and fails to identify the proposed combination with any specificity.

For these reasons, and those below, Patent Owner requests that the Board find Petitioners have failed to demonstrate that the challenged claims are unpatentable.

II. TECHNOLOGICAL BACKGROUND

A. The '035 Patent

The '035 Patent was filed on February 7, 2017 and is a continuation of U.S. Patent No. 9,563,587, which claims priority to U.S. Provisional Patent Application No. 61/676,883, filed on July 27, 2012. The '035 Patent generally relates to memory modules, and more particularly to multi-rank memory modules and methods of operation.

One embodiment of the invention includes a module control device 116, a plurality of buffer circuits 118, and memory devices 12 that are mounted on the memory module 110. Ex. 1001, 4:18-43; Ex. 2010, ¶ 24. The module control device 116 receives command and address signals from the off-module system memory controller 101 (4:63-5:8) and outputs module command signals and module control signals to the memory devices and the buffer circuits, respectively. Ex. 1001, 5:55-67; Ex. 2010, ¶ 24.

Figure 2A shows the logical interconnection of the aforementioned components, while Figure 2C shows the physical arrangement of the same components on the module.

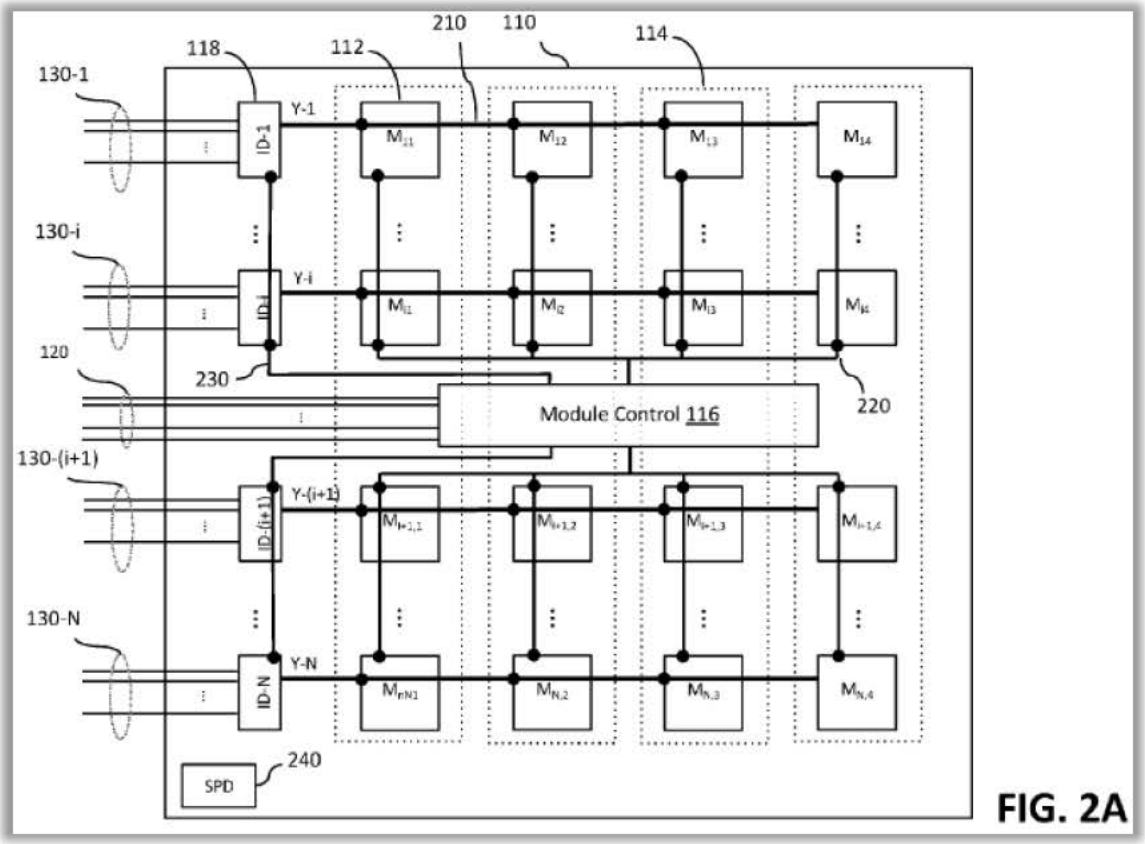
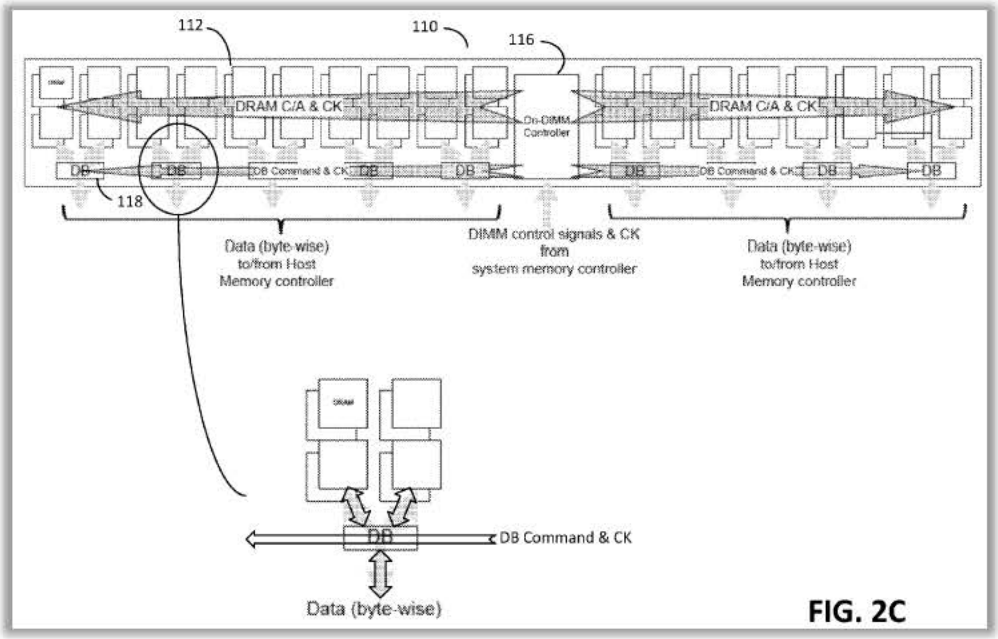


FIG. 2A

Ex. 1001, Fig. 2A; Ex. 2010, ¶ 25.



Ex. 1001, Fig. 2C; Ex. 2010, ¶ 25.

The '035 Patent describes the need to overcome limitations of prior art memory modules and the complications posed by increasing the number of memory devices—and thus the memory density—on the memory module. For example, the specification describes the limitations of conventional prior art read and write leveling mechanisms used to compensate for unbalanced wire lengths:

> In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure proper timing of the control and/or data signals received and/or transmitted by the memory modules.

Ex. 1001, 2:25-32; Ex. 2010, ¶ 26.

The '035 Patent teaches mechanisms for buffering command, address, timing, and data information via a module control device, a plurality of buffer circuits, and memory devices located on the memory module, resulting in modules with higher capacity and higher performance than in the prior art. The '035 Patent further discloses logic circuitry in the buffer circuits that is configured to obtain timing information based on signals received during one memory operation and, in accordance with such timing information, control the timing of data and strobe signals on the data paths in a subsequent memory operation. Ex. 1001, cl. 1; Ex. 2010, ¶ 27.

B. The Osanai Reference (Ex. 1005)

U.S. Patent Application No. 2010/0312925 A1 to Osanai et al. ("Osanai") is directed to a "Load Reduced memory module in which a considerably high data transfer rate can be realized" and includes a plurality of data register buffers, data connectors, and memory chips in a line along a memory module substrate. Ex. 1005, [0008], [0018]. In this way, "a line length from a data connector to a memory chip is considerably shortened," which "makes it possible to enhance the signal quality on the module substrate." Ex. 1005, [0018]; Ex. 2010, ¶ 29.

The components of memory module 100, shown in Figure 1, include the command/address/control register buffer 400, data register buffers 300, and memory chips 200. Ex. 1005, Fig. 1; Ex. 2010, ¶ 30. The singular command/address/control

register 400, detailed in Figure 6, receives commands sent from memory controller 12 over signal paths 23 (also called line L3). Ex. 1005, [0074-75], [0109], [0113], Figs. 1, 3, 6, 7; Ex. 2010, ¶ 30. From these commands, register device 400 generates control signals directed to data register buffer circuits 300 and memory chips 200. Ex. 1005, Figs. 1, 6; Ex. 2010, ¶ 30. Control signals exit the command register device 400 through ports 402 and 403 to reach the memory devices 200 and their corresponding data register buffers 300, respectively. Ex. 1005, [0120], [0113], Figs. 1, 7; Ex. 2010, ¶ 30.

Osanai's data register buffers 300 receive write data flowing from the off-module memory controller to the memory chips 200 and read data flowing from the memory chips to the memory controller. Ex. 1005, [0090-99], Fig. 5; Ex. 2010, ¶ 31. In both directions, the data is forwarded to the opposite interface and transmitted towards its destination. *Id.* In Osanai's modules, the data signals (DQ) are paralleled by a data strobe signal (DQS). Ex. 1005, [90]; Ex. 2010, ¶ 31.

Osanai describes read and write leveling operations to adjust write timing and to adapt to read timing, respectively, "in consideration of a propagation time of a signal." Ex. 1005, [0146]; Ex. 2010, ¶ 32. Osanai discloses that write leveling circuit 322 performs write leveling operations to match the phase of the strobe signal DQS to the clock signal CK at each memory chip 200. Ex. 1005, [0148-49]; Ex. 2010, ¶ 32. Osanai's command/address/control register buffer 400 supplies CK to both

data register buffers 300 and memory chips 200. Ex. 1005, [0148-49]; Ex. 2010, ¶ 32.

In Osanai's write leveling procedure, the write leveling circuit 322 in each of the data register buffers 300 adjusts the timing of data (DQ) and data strobe (DQS) signals so they arrive at memory chips 200 at precisely the correct time. Ex. 1005, [0096], [0146-52]; Ex. 2010, ¶ 33. During write leveling, the DLL circuit 310 is adjusted to set the proper phase between CK entering the buffer 300 and the local write clock LCLKW. Ex. 1005, [0090], [0093]. This clock determines when the FIFO (Write) 301 outputs data and when the strobe generating circuit 376 generates the corresponding transitions on the DQS signal. Ex. 1005, [0093-0094], [0096-97]; Ex. 2010, ¶ 33.

Osanai's read leveling operation determines when input buffers INB[1] are activated to receive read data signals and strobe signals coming from memory chips 200 over L1 and L2 via terminals 341, 342, 351, and 352. Ex 1005, [0146], [0153-57], Fig. 15; Ex. 2010, ¶ 34. A control signal from Data Register Control Circuit 320 turns on input buffers for signals DQS and DQ before the expected arrival of the

[1] The Petition improperly refers to INB and OUTB shown in Figure 5 of Osanai as signals. Pet., 33; Ex. 1003, ¶ 111. In fact, these annotations in Figure 5 point to input and output buffer **circuits**. Ex 1005, Fig. 5; *id.,* [0094]; Ex. 2010, ¶ 34 n.2.

data and strobe signals so they can pass through to the selectors and be captured by the FIFO (Read) circuit 302 according to the timing information provided by the corresponding strobe signal. Ex. 1005, Fig. 5, [0094], [0157]; Ex. 2010, ¶ 34; *see also* Ex. 2011, 76:21-77:4. Importantly, Osanai's read leveling only adjusts the timing of when the input buffers INB are turned on so they are active when data arrives; it does not adjust the timing of any data or data strobe signal on the bus or within the buffer:

> The read data DQ output from the memory chip **200** reaches the data register buffer **300**, by which the data register buffer **300** can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is … used in an adjustment of an activation timing of the input buffer circuit INB and the like.

Ex 1005, [0157]; Ex. 2010, ¶ 34. Petitioners' expert agreed that the purpose of read leveling as disclosed in Osanai is to adjust the timing of the activation of input buffers INB. *See* Ex. 2011, 76:22-77:4.

Osanai's data register buffer 300 includes FIFO (Read) circuit 302 and FIFO (Write) circuit 301. Ex. 1005, Fig. 5, [0090-91]. Ex. 2010, ¶ 37. The decoupling of the insertion and extraction of data into the FIFOs is important for proper operation of Osanai's buffer 300. Ex. 2010, ¶ 37.

Osanai does not disclose that any "*timing information*" is obtained "*during a second memory operation prior to the first memory operation*." Pet., 36.

C. The Tokuhiro Reference (Ex. 1006)

U.S. Patent No. 8,020,022 to Tokuhiro ("Tokuhiro") discloses a system that detects time delays during known write leveling procedures and applies such delay to adjust strobe signals sent from the system memory controller to a memory module during a write operation. Ex. 1006, 3:16-26. Tokuhiro proposed an improved memory controller whereby such time delay determined for the strobe signals during write leveling can be used to compute similar adjustments for the data signals received from respective SDRAMs of the memory module during a read operation. Ex. 1006, 2:54-59, 13:66-14:6, equations (1), (2-1)-(2-3), (3-1)-(3-6); Ex. 2010, ¶ 38. As such, Tokuhiro does not suggest any changes or improvements to the components on the memory module, but only to the off-module memory controller and the controlling structures on the CPU. Ex. 1006, Fig. 4-6, 2:16-26; Ex. 2010, ¶ 38. Tokuhiro discloses a fly-by topology for wiring between the memory controller 12 and the SDRAM devices mounted on DIMM module 11. Ex. 1006, 5:24-30; Ex. 2010, ¶ 38.

Importantly, Tokuhiro describes and incorporates known write leveling mechanisms, as disclosed in the Joint Electron Device Engineering Counsel

("JEDEC") DDR3 SDRAM Standard, JESD79-3. Ex. 1006, 1:22-32; 2:10-12; 2:46-49; 2:54-59; Ex. 2010, ¶ 39. Tokuhiro describes such mechanisms as follows:

> The term "write leveling function" refers to the function of sampling the clock signal CK by using the data strobe signal DQS output from the memory controller 90, detecting the phase relationship between the data strobe signal DQS and the clock signal CK, and adjusting (compensating) a delay time of the data strobe signal DQS.

Ex. 1006, 2:13-18; Ex. 2010, ¶ 39.

In this way, "the difference in the delay time caused in the write operations between the memory controller . . . and the plurality of SDRAMS . . . is adjusted by employing the write leveling function." Ex. 1006, 2:46-49; Ex. 2010, ¶ 40. Tokuhiro describes that, once write leveling is complete, strobe signals and clock signal from the system memory controller will arrive at respective SDRAMs on the memory module at substantially the same time. Ex. 2006, 2:39-45, 12:59-63; Ex. 2010, ¶ 40. Tokuhiro notes that, although the JEDEC DDR3 standards specified such write leveling procedures for write operations, "compensations of the signal arrival time in read operations are not provided with the JEDEC standards." Ex. 1006, 2:54-59; Ex. 2010, ¶ 40.

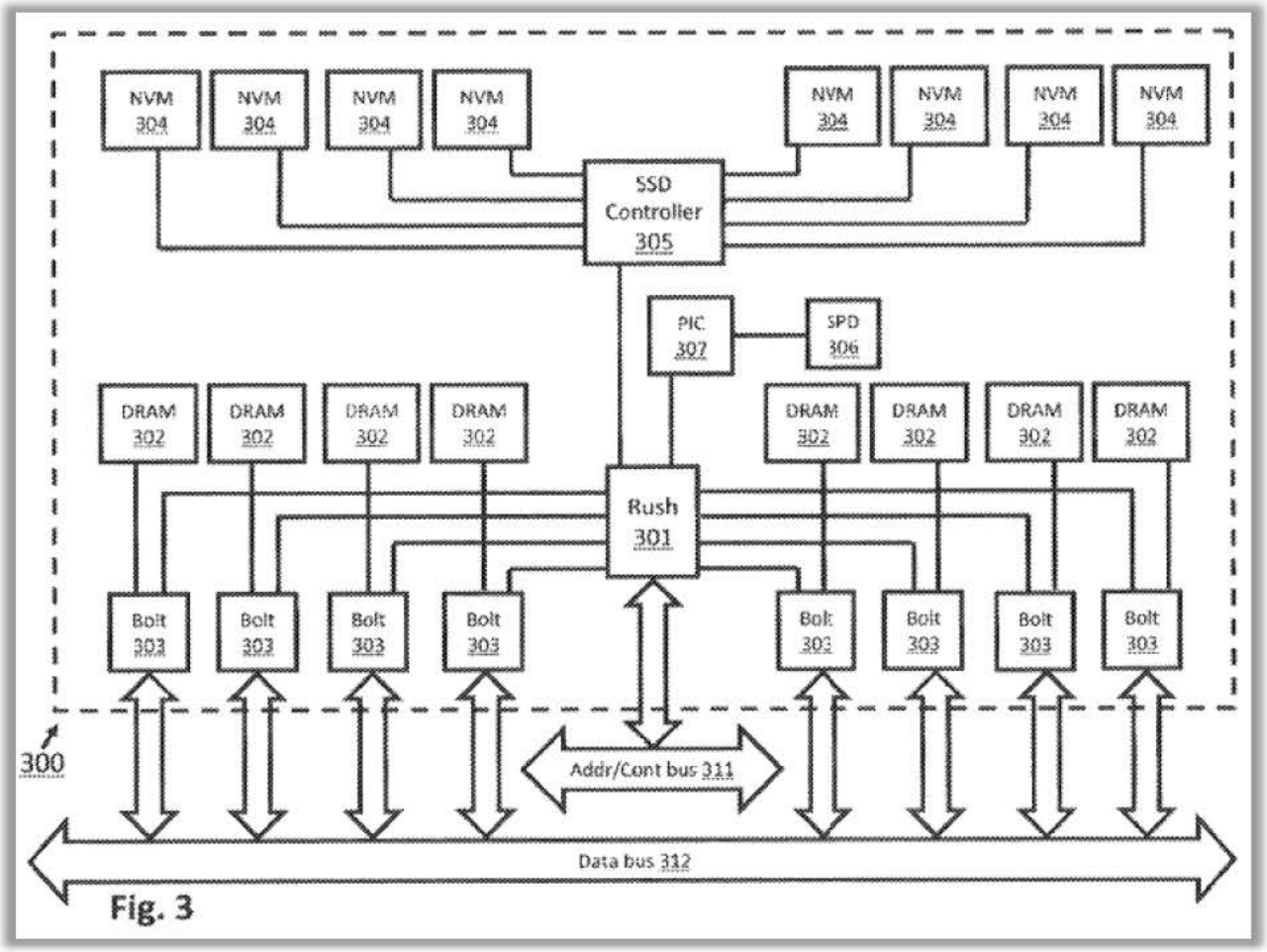
Accordingly, Tokuhiro focuses on using delays detected by the known JEDEC write leveling procedure to compute time delays for compensating signals during read operations. Ex. 2010, ¶ 41.

Tokuhiro acknowledges that the write leveling function and variable delay circuits—which can change respective delay times of the data strobe signals—are present in the prior art and that their use in a system memory controller is not novel. Ex. 1006, 1:34-2:49, Fig. 2; Ex. 2010, ¶ 42.

D. The Takefman Reference (Ex. 1007)

U.S. Patent No. 8,713,379 to Takefman et al. ("Takefman") discloses a system including a computer processing unit ("CPU"), a memory module, and memory bus connecting the CPU and the memory module, as well as a co-processing unit (or input/output device). Ex. 1007, 1:48-55; Ex. 2010, ¶ 43.

Takefman discloses a TeraDIMM architecture embodiment including a module controller ("Rush") 301, a number of DRAM devices 302, a number of data buffer ("Bolt") devices 303, a rank of non-volatile memory devices 304, an SSD controller 305, an SPD 306, and a PIC microcontroller 307. Ex. 1007, 5:53-6:13; Ex. 2010, ¶ 44. In this embodiment, data exchanged between the data bus and the DRAMs 302 flow exclusively through Bolt devices 30, while commands to the DRAMs 302 flow through Rush 301 on their way to the DRAMs 302. Ex. 1007, 5:53-6:13, Fig. 3; Ex. 2010, ¶ 44. Significantly, Takefman does not teach that Rush 301 communicates directly with or sends signals to DRAMs 302. Ex. 2010, ¶ 44.



Ex. 1007, Fig. 3; Ex. 2010, ¶ 44.

Takefman's Rush 301 includes per-lane delay compensation circuits that allow for programmable launch times and lane de-skew on receipt from the Bolt 303 devices 303. Ex. 1007, 6:14-26; Ex. 2010, ¶ 45. Takefman does not disclose that Bolt devices 303 include any delay compensation circuit, or that they obtain timing information based on signals they receive. Ex. 2010, ¶ 45.

III. LEVEL OF ORDINARY SKILL

While Patent Owner disputes Petitioners' definition of the level of a person of ordinary skill in the art ("POSITA"), resolution of such dispute is not necessary for the Board to decide the validity of the challenged claims.

IV. CLAIM CONSTRUCTION

The '035 Patent's challenged claims are to be construed "using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)." 37 C.F.R. § 42.100(b) (Nov. 13, 2018). Petitioners do not seek construction of any terms in the '035 Patent, and, for this filing, neither does Patent Owner. For purposes of this Response only, Patent Owner agrees with Petitioners that all terms of the '035 Patent have their plain and ordinary meaning.

V. PETITIONERS HAVE FAILED TO DEMONSTRATE THAT THE CHALLENGED CLAIMS ARE OBVIOUS

A. All Grounds: Petitioners fail to provide evidence that any reference discloses or suggests "*obtain[ing] timing information*" as claimed (all claims).

All asserted Grounds suffer the same facial deficiency: Tokuhiro does not disclose "*obtain[ing] timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*." Ex. 1001, cl. 1. Indeed, Tokuhiro teaches that during the write leveling function, which Petitioners identify as purportedly satisfying this claim element, **no memory operations can be performed at all**. Thus, Tokuhiro's

write leveling function identified by Petitioners does not satisfy the claims' requirement that "*timing information*" be "*obtain[ed]*" "*during a second memory operation*." For this reason, the Petition fails.

1. Petitioners concede that neither Osanai, nor Takefman discloses or suggests "*obtain[ing] timing information.*"

Claim 1 of the '035 Patent (and all dependent claims) requires buffer circuits to include "*logic . . . configured to obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information*." Ex. 1001, cl. 1.

Petitioners concede that Osanai does not teach, disclose, or suggest logic configured to "*obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*." Pet., 36 ("But Osanai does not explicitly disclose that the timing information is obtained '*during a second memory operation prior to the first memory operation*.'") (emphasis in original).

Petitioners also concede that Takefman does not teach, disclose, or suggest logic configured to "*obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*." Pet., 63 ("Takefman . . . does not expressly

disclose that the timing information is obtained '*during a second memory operation prior to the first memory operation*.'") (emphasis in original).

2. Tokuhiro only discloses the method of write leveling already considered in the '035 Patent specification.

For all three Grounds, Petitioners point solely to Tokuhiro's write leveling function as purportedly satisfying the "*obtain timing information"* element. Pet., 36-38, 63-66, 70-71. Specifically, Petitioners state that Tokuhiro discloses write leveling techniques, which are necessary to compensate for different propagation delays caused by memory units with different wiring lengths. Pet., 36. Petitioners point to the following passage in Tokuhiro, which discusses a time delay determined using a known, standardized method of write leveling:

> In other words, the second delay time Dt2 for the data signal DQ input from the SDRAM can be calculated by using the first delay time Dt1 that has been set in the write leveling. Accordingly, in the second delay time control unit 24, the second delay time Dt2-x corresponding to one SDRAM-x is set by using the above-mentioned formula (3-5) so that the sum of the first delay time Dt1-x and the second delay time Dt2-x both corresponding to the relevant SDRAM-x is equal to a preset value.

Id., 37 (citing Ex. 1006, 16:1-28).

As an initial matter, the Petition fails to prove that Tokuhiro's calculation of delay time Dt2 using a first delay time Dt1 that is "set in the write leveling" satisfies the claims' requirement that timing information obtained be "*based on one or more*

signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation." *See* Pet., 37. Petitioners do not show that Tokuhiro's delay time Dt1 is obtained based on signals received by the buffer circuit "*during a second memory operation prior to the first memory operation*." Instead, Petitioners point only to a delay determined during a ***write leveling procedure*** and then summarily—and incorrectly—conclude that such determination means that the delay was determined "*during a second memory operation*." Pet., 37 ("Consequently, Tokuhiro teaches a delay unit that obtains a first delay time from a write operation ('*during a second memory operation*') . . . For example, Tokuhiro discloses calculating a second delay time for the read operation based on the first delay time determined by the write level operation.") (emphasis in original). But Petitioners have not shown that Tokuhiro's write leveling procedure—during which such delay is determined—is a claimed "*second memory operation*." This constitutes a threshold failure of proof. And even if Petitioners had attempted to show that Tokuhiro teaches obtaining timing information "*during a second memory operation,*" they could not, as described in detail below.

Tokuhiro makes clear that write leveling mechanisms were already known to a POSITA, as detailed in the JEDEC DDR3 standard, JESD79-3.[2] *See id.,* 1:22-26 ("Recently, the DDR3 . . . memory interface has been standardized as standards of a DRAM . . . by JEDEC . . . (*see*, *e.g.*, JDEC STANDARD (JESD79-3; DDR3

[2] JEDEC's JESD79-3 was published in June 2007. *See* Ex. 2013, JEDEC Standard DDR3 SDRAM Standard JESD79-3 (June 2007). JESD79-3A, the first revision of JESD79-3, was published in September 2007. *See* Ex. 2014, JEDEC Standard DDR3 SDRAM Specification JESD79-3A (September 2007). Tokuhiro was filed on September 12, 2008; thus, references in Tokuhiro to "JESD79-3" should be interpreted as including the standard as originally published and all supplements available at the time of Tokuhiro's filing. *See* Ex. 2010, ¶ 67. Petitioners' expert agreed. *See* Ex. 2011, 42:17-22, 47:11-48:15. Thus, citations to JESD79-3 hereinafter will be to JESD79-3A. However, there are no material differences between JESD79-3 and JESD 79-3A, and citations to both versions are included herein for the Board's consideration. *See* Ex. 2010, ¶ 67; *see also* Ex. 2011, 51:1-7 ("Q. Sitting here today, are you aware of any distinctions between JESD79-3 as originally published and any of these subsequent revisions that relate to write leveling specifically? A. Not that I can recall, no."). Petitioners rely on and cite to JEDEC's JESD79-3C, published November 2008. *See* Ex. 1013.

SDRAM Standard)).”); *see also id.,* 2:10-45 (“For that reason, ***according to the JEDEC standards***, it is specified to employ the write leveling function ***in the DDR3 memory interface***.”) (emphasis added); *see* Ex. 2010, ¶ 66.

Tokuhiro does not purport to teach improvements to the JEDEC write leveling mechanisms, which Petitioners’ expert, Dr. Donald Alpert (“Dr. Alpert”) conceded in his deposition. *See* Ex. 2010, ¶ 68; *see also* Ex. 2011, 101:18-21 (“Q. You’re not offering any opinion that Tokuhiro teaches write leveling other than what is disclosed in DDR3 standard JESD79-3? A. That’s correct.”). Instead, acknowledging that JEDEC had already specified procedures for write leveling that were known at the time, Tokuhiro sought to improve the management of the read path in the memory controller by setting a second variable delay unit in the read data path within the memory controller 12, whereby the second delay time is set based on the first delay time. Ex. 1006, 3:24-26; *id.,* 2:54-59 (“Although, the DDR3 memory interface compensates the arrival time . . . in the write operations ***according to the JEDEC standards as described above***, compensations of the signal arrival time in read operations are not provided with the JEDEC standards.”) (emphasis added); *see* Ex. 2010, ¶ 68. Critically, none of Petitioners’ cited passages from Tokuhiro identify any improvements to the JEDEC DDR3 write leveling functionality. *See generally* Pet., 36-38; *see* Ex. 2010, ¶ 68. Dr. Alpert does not dispute that Tokuhiro merely discloses known JEDEC-compliant write leveling. Ex.

2011, 101:18-21 ("Q. You're not offering any opinion that Tokuhiro teaches write leveling other than what is disclosed in DDR3 standard JESD79-3? A. That's correct.").

The '035 Patent specification also identifies ***the same write leveling functionality described as known in Tokuhiro*** as prior art:

> In some conventional memory systems, the memory controllers include leveling mechanisms for write and/or read operations to compensate for unbalanced wire lengths and memory device loading on the memory module. As memory operating speed and memory density continue to increase, however, such leveling mechanisms are also insufficient to insure [sic] proper timing of the control and/or data signals received and/or transmitted by the memory modules.

Ex. 1001, 2:25-32; Ex. 2014, 38-41, Ex. 2013, 38-41; *see* Ex. 2010, ¶ 70.

Just as in Tokuhiro, the '035 Patent states that such write leveling mechanisms are used "to compensate for unbalanced wire lengths." Ex. 1001, 2:25-32; *see also* Ex. 1006, 1:63-2:9; *see* Ex. 2010, ¶ 70. Unlike Tokuhiro, however, the '035 Patent recognizes that such write leveling mechanisms are "insufficient to insure [sic] proper timing of the control and/or data signals received and/or transmitted by the memory modules" for the modules disclosed, and proposes the claimed solution. Ex. 1001, 2:25-32; *see* Ex. 2010, ¶ 70.

Thus, the known JEDEC DDR3 write leveling functionality is Petitioners' only cited support for their assertion that Tokuhiro meets the Petitioners' only cited

support for their assertion that Tokuhiro meets the "*obtain timing information*" "*during a second memory operation*" limitation. Pet., 36-38; *see also* Ex. 2011, 117:12-21 ("Q. [S]itting here today, you don't intend to opine that some other calculation of timing information disclosed in Tokuhiro satisfies this obtained timing information limitation we've been discussing, correct? . . . A. Well, I'm not offering another opinion now."). And as explained below, the JEDEC DDR3 write leveling functionality does not obtain timing information "*based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*" as required in claim 1 of the '035 Patent.

3. Tokuhiro does not disclose or suggest "*obtain[ing] timing information*" "*during a second memory operation*" as claimed.

The JEDEC DDR3 standard, which Tokuhiro identifies as teaching a known write leveling method, describes a write leveling procedure that is performed by the system memory controller to align strobe (DQS) and clock (CK) signals arriving at each memory device located on a DDR3 memory module. *See* Ex. 2014, 38-41; *see* Ex. 2010, ¶ 74.[3] Once aligned during the write leveling process, this timing is subsequently used during write operations to delay the data and strobe signals so that

[3] *See* Ex. 2013, 38-41.

they arrive at the SDRAMs at a time when the SDRAMs can reliably capture the write data:

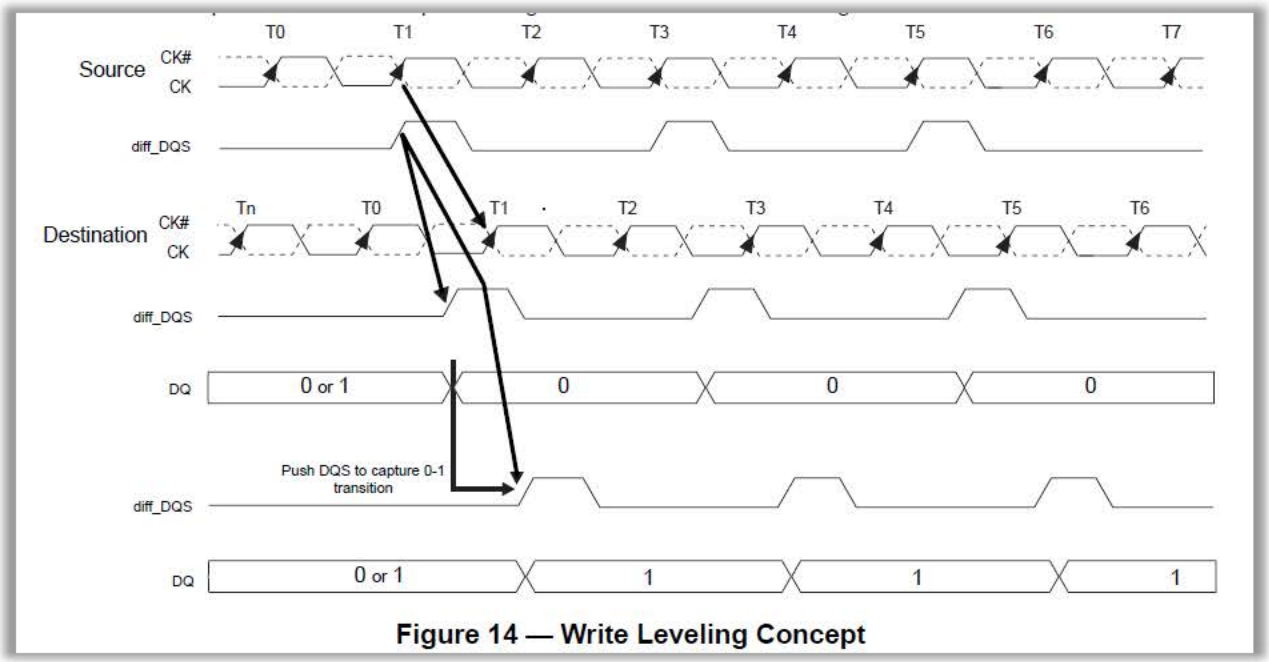


Figure 14 — Write Leveling Concept

See Ex. 2014, Fig. 14 (September 2007); *see* Ex. 2010, ¶ 74.[4] As described in JESD79-3A, the write leveling mode of operation ("Write Leveling Mode") is enabled or disabled using a Mode Register Set (MRS) command. Ex. 2014, 41; *see* Ex. 2010, ¶ 75.[5]

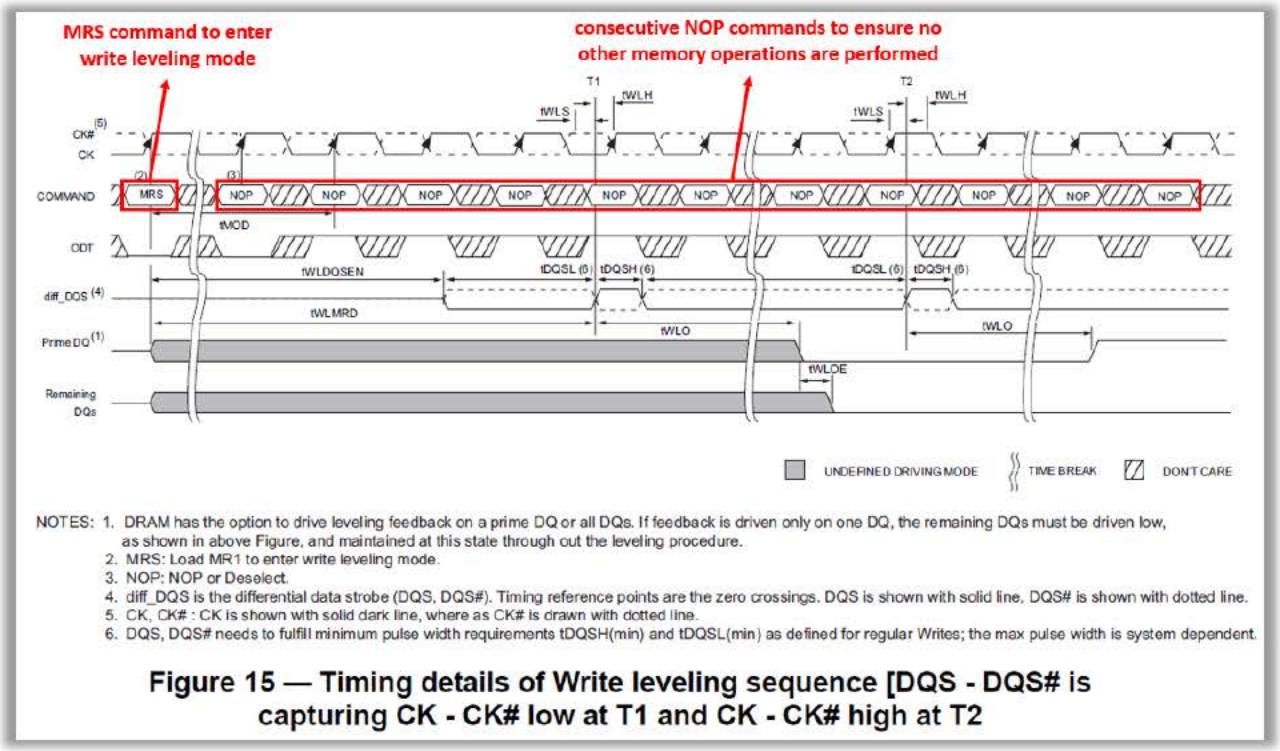
Importantly, however, during the Write Leveling Mode, JESD79-3 teaches that the memory module is **prohibited** from performing any memory operations at

[4] *See* Ex. 2013, Fig. 14 ("Write leveling concept").

[5] *See* Ex. 2013, 41 ("After the RTT is switched off, disable Write Level Mode via MR command").

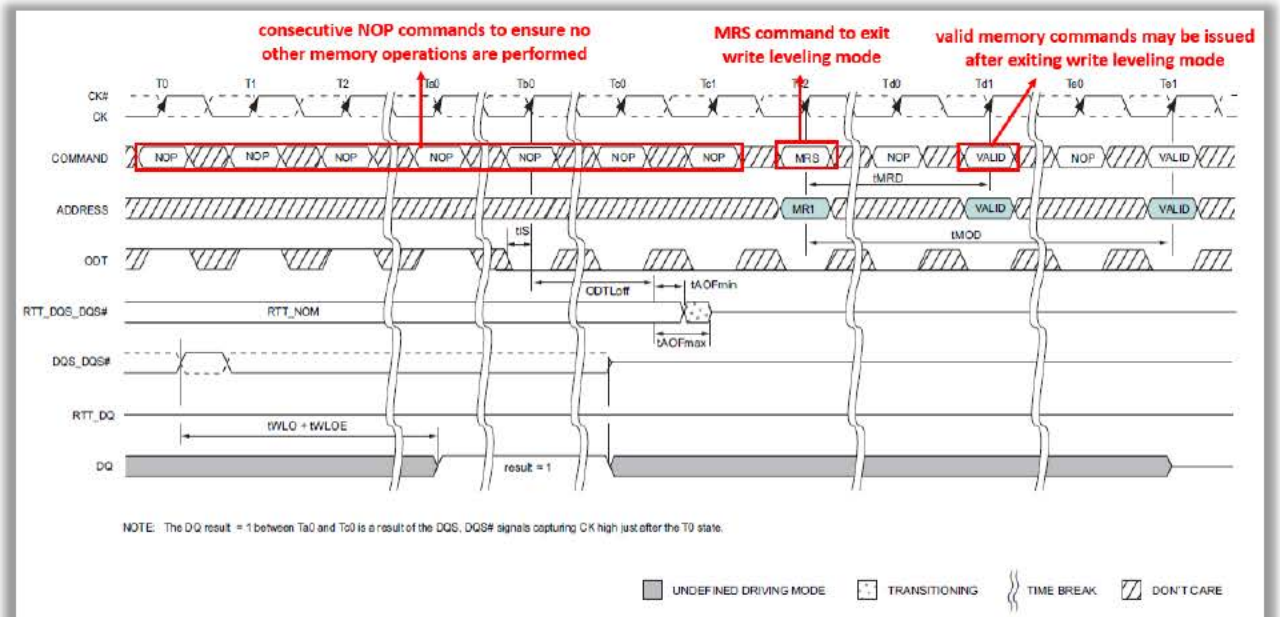
the direction of the memory controller, or otherwise. For example, JESD79-3A states that, "[w]ith entering write leveling mode, the DQ pins are in undefined driving mode. ***During write leveling mode, only NOP or DESELECT commands are allowed, as well as an MRS command to exit write leveling mode***." Ex. 2014, 39 (emphasis added); *see* Ex. 2010, ¶ 75.[6] Timing diagrams confirm that the system memory controller sends consecutive NOP commands to ensure that the memory controller does not issue any other memory operations until after issuing the MRS command to exit the write leveling procedure:

[6] *See* Ex. 2013, 39 ("With entering write leveling mode, the DQ pins are in undefined driving mode. During write leveling mode, only NOP or DESELECT commands are allowed.").



NOTES: 1. DRAM has the option to drive leveling feedback on a prime DQ or all DQs. If feedback is driven only on one DQ, the remaining DQs must be driven low, as shown in above Figure, and maintained at this state through out the leveling procedure.
2. MRS: Load MR1 to enter write leveling mode.
3. NOP: NOP or Deselect.
4. diff_DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. DQS is shown with solid line, DQS# is shown with dotted line.
5. CK, CK# : CK is shown with solid dark line, where as CK# is drawn with dotted line.
6. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH(min) and tDQSL(min) as defined for regular Writes; the max pulse width is system dependent.

Figure 15 — Timing details of Write leveling sequence [DQS - DQS# is capturing CK - CK# low at T1 and CK - CK# high at T2



NOTE: The DQ result = 1 between Ta0 and Tc0 is a result of the DQS, DQS# signals capturing CK high just after the T0 state.

Figure 16 — Timing details of Write leveling exit

Ex. 2014, Figs. 15, 16 (annotated); *see* Ex. 2010, ¶ 76.[7] As shown in JESD 79-3A, no commands other than NOP and DESELECT commands can be issued until the Write Leveling Mode has been exited via an MRS command. *See* Ex. 2014, Fig. 15; *see* Ex. 2010, ¶ 76.[8]

None of the commands that are issued during Write Leveling Mode, including NOP and DESELECT commands, are "*memory operations*" under a plain and ordinary meaning of the term as understood by a POSITA. *See* Ex. 2010, ¶ 77. NOP, short for "no operations," is a null command that does not instruct the memory device to do anything. Ex. 2014, 29-30, 32;[9] *see* Ex. 2010, ¶ 78. DESELECT commands, also called "device deselected" commands, are indicated by the chip select input (CS#) being unasserted, which causes the SDRAM to ignore other command and address inputs. *See* Ex. 2010, ¶ 78. As with NOP commands, no operations will be performed when the DESELECT command is presented to the SDRAM. *See* Ex. 2010, ¶ 78. Mode Register Set ("MRS") commands, used to enter and exit Write Leveling Mode, are also not "*memory operations*" under a plain and ordinary meaning of the term as understood by a POSITA. *See* Ex. 2010, ¶ 79. Mode

[7] *See* Ex. 2013, Figs. 15, 16.

[8] *See* Ex. 2013, Fig. 15.

[9] *See* Ex. 2013, 30, 32.

Register Set Commands transfer the contents of the address input to a specified mode register to affect device operation—they do not affect the memory portion of the SDRAM. *See* Ex. 2010, ¶ 79. Specifically, the MRS commands that enter or exit Write Leveling Mode set or clear the Write Leveling Enable bit in Mode Register 1 (MR1). Ex. 2014, 22-23, 39-41;[10] *see* Ex. 2010, ¶ 79.

Because none of the commands issued during Write Leveling Mode are memory operations, it is only upon exiting the Write Leveling Mode that any memory operation (*e.g.,* a memory read, write, or activate operation) can be performed. *See id.,* Fig. 16; *see* Ex. 2010, ¶ 80.[11]

JESD 79-3A's Simplified State Diagram Figure 1 confirms that no "*memory operations*" as claimed are performed during Write Leveling Mode. *See* Ex. 2014, Fig. 1;[12] *see* Ex. 2010, ¶ 81. Figure 1 shows a simplified state diagram of a DDR3 SDRAM wherein the write leveling procedure can only be entered from an idle state. *See* Ex. 2014, Fig. 1; [13] *see* Ex. 2010, ¶ 81. Upon exiting the Write Leveling Mode, the memory device returns to an idle state from which a memory read or write

[10] *See* Ex. 2013, 22-23, 39-41.

[11] *See* Ex. 2013, Fig. 16.

[12] *See* Ex. 2013, Fig. 1.

[13] *See* Ex. 2013, Fig. 1.

operation can only be performed once the memory device enters an active state using an ACT (*e.g.*, Activate) command. *See* Ex. 2014, Fig. 1; [14] *see* Ex. 2010, ¶ 81.

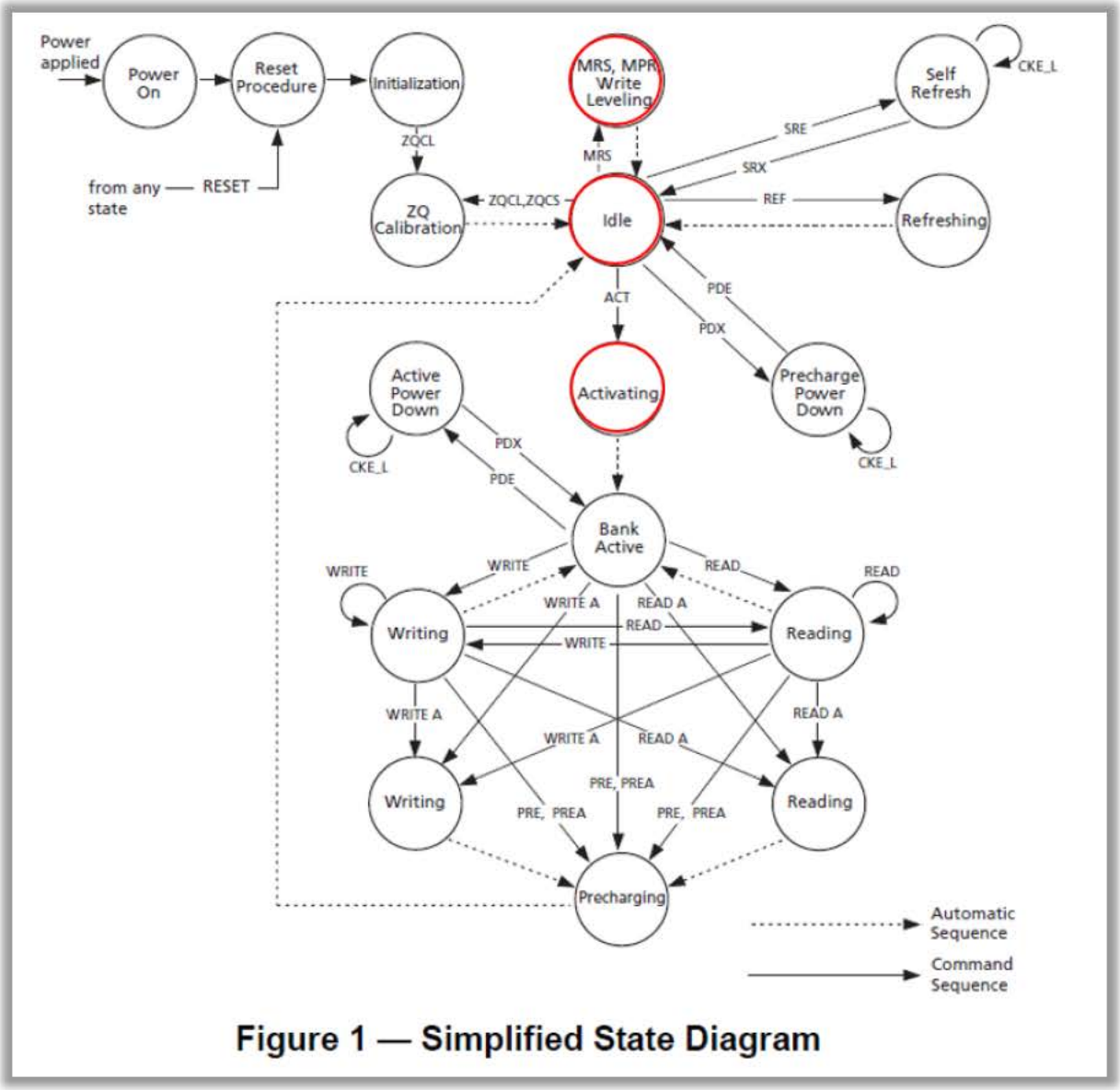


Figure 1 — Simplified State Diagram

See also Ex. 2014., Fig. 1 (annotated); *see* Ex. 2010, ¶ 81.[15]

[14] *See* Ex. 2013, Fig. 1.

[15] *See* Ex. 2013, Fig. 1.

Tokuhiro discloses how delay time Dt2 in the read path can be determined from the first delay time Dt1 "that has been set in the write leveling." Pet., 37; *see* Ex. 2010, ¶ 82. As described above, however, any delay time set in Write Leveling Mode is not "*timing information*" obtained "*during a . . . memory operation*" as claimed because, as Tokuhiro and JESD79-3 teach, no memory operations can be performed during write leveling. *See* Ex. 2010, ¶ 82.

Petitioners use the terms "write leveling operation" and "write operation" interchangeably in certain instances, improperly suggesting that the write leveling operation is a write operation and, therefore, a memory operation. *See*, *e.g.*, Pet., 37 (explaining that "Tokuhiro teaches a delay unit that obtains a first delay time from a **write operation**" because "Tokuhiro discloses calculating a second delay time for the read operation based on the first delay time determined by the **write level operation**") (emphases added). But Petitioners are wrong; the terms "write leveling" and "write operation" are not synonymous—which Petitioners' own expert conceded—and the write leveling procedure as taught by Tokuhiro is *not* a write operation and does not include a write operation, as that term would be understood by a POSITA at the time of the invention. *See Ex*. 2011, 118:7-13 ("Q. You agree that there is a distinction between a write operation and a write leveling procedure? . . . A. Yes."); *see also id.*, 150:17-21 ("Q. What did you understand the term 'write operation' to mean in that question? A. Well, I thought that write operation would

generally mean an operation that relates to writing to the memory."); *see* Ex. 2010, ¶¶ 83-84.

As described above, *no* memory operations, including write operations, may be performed during Tokuhiro's write leveling procedure, and none of the commands issued during Write Leveling Mode are claimed "*memory operations*" under a plain and ordinary meaning of the term as understood by a POSITA. It is only once the write leveling procedure is complete can any memory operation, including write operations, be performed. *See* Ex. 2014, Fig. 16; *see* Ex. 2010, ¶ 85.[16] Petitioners' imprecise use of language is misleading at best and distorts Tokuhiro's teachings.

The Board's Institution Decision asks whether Tokuhiro's write leveling procedure nevertheless teaches the recited "*second memory operation*" even though other memory operations are prohibited from being performed during the procedure. Paper 16, 26. As described above, under the plain and ordinary meaning of the claim language as understood by a POSITA, the answer is clearly "no." Any timing information determined ***during*** Tokuhiro's write leveling is not "*obtain[ed]*" during a "*second memory operation*" as required by the challenged claims. As a result, Tokuhiro does not disclose or suggest a buffer circuit including logic configured to

[16] Ex. 2013, Fig. 16.

"*obtain timing information based on one or more signals received by the each respective buffer circuit* ***during a second memory operation*** *prior to the first memory operation*." Ex. 1001, cl. 1 (emphasis added); *see* Ex. 2010, ¶ 86. All Grounds fail as a result.

B. Ground 1: Petitioners' proposed combination of Osanai and Tokuhiro does not disclose all limitations of the challenged claims.

1. Petitioners fail to provide evidence that any reference discloses or suggests "*logic . . . further configured to . . . control timing of the respective data and strobe signals on the data paths in accordance with the timing information*" as claimed (all claims).

The Petition suffers from a wholesale failure of proof for Ground 1, as Petitioners have failed to identify where the proposed combination of Osanai and Tokuhiro discloses "*logic . . . further configured to . . . control timing of the respective data and strobe signals on the data paths in accordance with the timing information*."

Claim 1 of the '035 Patent discloses "*logic*" that is configured to perform three functions:

(1) "*respond to the module control signals by enabling the data paths*";

(2) "*obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*,"; and

(3) "*control timing of the respective data and strobe signals on the data paths in accordance with the timing information*."

Ex. 1001, cl. 1. As established herein, Petitioners proffered proof for the claimed "*logic*" is unavailing. Indeed, Petitioners do not even attempt to show that either Osanai or Tokuhiro disclose the "*control timing*" element. Thus, the Petition does not adequately show that this claim element is met. For this reason alone, the Petition fails.

a. Petitioners summarily allege that Osanai teaches "*logic*" configured to "*control timing . . . of the respective data and strobe signals on the data paths in accordance with the timing information*."

In a heading, Petitioners summarily assert that Osanai discloses this claim element. Pet., 34 ("Osanai discloses "*logic [that] is further configured to obtain timing information based on one or more signals received by the each respective buffer circuit*" used "*to control timing of the respective data and strobe signal on the data paths in accordance with the timing information*.") (emphasis and alterations in original). Under this heading, Petitioners describe Osanai's read and write leveling procedures, which, Petitioners argue, "make timing adjustments so that signals between 'the memory chips 200 and the data register buffer 300' are sent at the appropriate time." Pet., 34. Petitioners also allege that, to make these adjustments, the read and write leveling circuitry uses the module clock (CK) signal set from the command/address/control register buffer and that, based on this clock signal, a "timing adjustment" is used to create DQ-Post and DQS-Post. *Id.* In doing

so, Petitioners assert, the leveling circuitry "adjust[s] a write timing or read timing in consideration of a propagation time of a signal." *Id.*

b. Petitioners do not identify where Osanai teaches "*control [of] timing*" (1) "*of the respective data and strobe signals*" (2) "*on the data paths*" (3) "*in accordance with the timing information*."

But this is the sum total of Petitioners' argument for this claim element. Nowhere in the Petition—other than in a heading—do Petitioners assert that Osanai discloses control of timing (1) of "*the respective data and strobe signals*" (2) "*on the data paths*" (3) "*in accordance with the timing information*," let alone show **where** Osanai discloses such requirements. *See* Ex. 1001, cl. 1.

Importantly, by the express claim language the "*data paths*" must be "*for transmitting respective data and strobe signals associated with the first memory operation.*" Ex. 1001, cl. 1. Although Petitioners allege that Osanai discloses "*data paths*" L1 and L2 inside data register buffer 300, Petitioners do not assert that Osanai discloses the claimed "*control*" of "*timing*" of data and strobe signals **on** L1 and L2—the purported "*data paths*"—for transmitting data and strobe signals associated with "*the first memory operation*," which Petitioners have expressly asserted is "the read operation." Pet., 37.

The only relevant analysis Petitioners include that might possibly relate to a read operation appears in Dr. Alpert's declaration, where he states summarily that "[a] similar read leveling process results in signals being delayed." Ex. 1013, ¶ 117.

But arguments made in a declaration, and not in the petition itself, cannot be considered. *Instrumentation Lab. Co. v. HemoSonics LLC*, IPR2017-00855, Paper 5, 20 (P.T.A.B. Feb. 13, 2019) ("[W]e decline to consider information that Petitioner does not discuss sufficiently in the Petition, but instead simply incorporates by reference to cited portions of the Mize Declaration."). And even if arguments made solely in an expert declaration can be considered, Dr. Alpert does not allege, as the claims require, that Osanai discloses "*control*" of "*timing*" of "*data and strobe signals*" across L1 or L2—or any other data path—for transmitting respective data and strobe signals associated with a read operation "*in accordance with the timing information*" obtained by the buffer's logic. *See id.*

This is a fundamental failure of proof for Ground 1. *See Nuevolution v. Chemgene Holdings APS*, IPR2017-01598, Paper 16, 35 (P.T.A.B. Jan. 11, 2018) ("Here again, Petitioner fails to address sufficiently the limitations of claims 1 and 5 requiring synthesis in the same reaction well, which we are not persuaded are taught or suggested in Pedersen."); *R.J. Reynolds Vapor Co. v. Fontem Holdings 1 B.V.*, IPR2018-00629, Paper 10, 13 (P.T.A.B. Aug. 29, 2018) ("Petitioner must explain with particularity how each element of the challenged claim is disclosed or rendered unpatentable by the prior art or the combination of the prior art upon which Petitioner relies."); 35 U.S.C. § 322(a)(3) (requiring a petition to identify "with particularity, each claim challenged, the grounds on which the challenge to each

claim is based, and the evidence that supports the grounds for the challenge to each claim"); 37 C.F.R. §§ 42.22(a)(2) (requiring a petition to include a "full statement of the reasons for the relief requested, including a detailed explanation of the significance of the evidence"), 42.104(b)(4) ("The petition must specify where each element of the claim is found in the prior art.").

c. Osanai does not teach that read leveling is used to "*control timing . . . of the respective data and strobe signals on the data paths in accordance with the timing information*."

Nor could Petitioners have credibly argued that Osanai teaches this claim limitation. The claims specifically require "*control*" of "*timing*" of "*data and strobe signals*" "*on the data paths*"—which must be "*for transmitting respective data and strobe signals associated with the first memory operation*"—"*in accordance with the timing information*." Ex. 1001, cl. 1. But Osanai does not teach that read leveling is used to "*control timing . . . of the respective data and strobe signals on the data paths in accordance with the timing information*."

Instead, Osanai's read leveling process delays the internal signal that turns on input buffers INB. *See* Ex. 1005, Fig. 5, [0034], [0154-57] ("The read data DQ output from the memory chip 200 reaches the data register buffer 300, by which the data register buffer 300 can find a time A from an input timing of the read command Read that is input as a part of the control signal DRC until the read data DQ is input. The time is measured for each of the memory chips 200, stored in the data register

control circuit 320 in the data register buffer 300, **and used in an adjustment of an activation timing of the input buffer circuit INB** and the like.") (emphasis added); *see* Ex. 2010, ¶ 104. During read leveling, read operations are performed with alternating bit patterns so that the data register buffer 300 can determine in which cycle the read data arrives from memory chips 200. Ex. 1005, [0157]; Ex. 2010, ¶ 105. As shown in Osanai's Figure 15, because of flight time delays, the read data might arrive at one data register buffer chip at a later time than the corresponding data would arrive at a second data register buffer chip on the same module. *See* Ex. 1005, Fig. 15; Ex. 2010, ¶ 105. Accordingly, the purpose of Osanai's read leveling is to allow the data register buffers 300 to turn on their INB input buffers connected to the L1 and L2 buses in time for them to receive the incoming data from the memory chips 200. Ex. 1005, [0157] ("The time is measured for each of the memory chips 200 . . . and used in an adjustment of an activation timing of the input buffer circuit INB"); Ex. 2010, ¶ 105. Osanai does not disclose read leveling for the purpose of adjusting the timing of the read data signals, themselves, which Petitioners' expert conceded in his deposition. *See* Ex. 2010, ¶ 105; *see also* Ex. 2011, 76:22-77:4 ("Q. The read leveling in Osanai as between data register buffer 300 and memory chip 200, adjusts when Osanai's input buffers INB, are turned on so that they're active when read data arrives, correct? A. Yes, that's correct."); *see also id.*, 90:6-17 ("Q. The activation of timing of the input buffer is not the same thing as a delay in the

output of the read data from the DRAM; correct? A. Yes. That's correct. The read leveling . . . doesn't change the timing for the DRAM to output its data."); *see also id.*, 91:5-17.

Moreover, the paths on which the INB input buffer control signals travel are not "*data paths*" on which data and strobe signals associated with a read operation are transmitted, and Petitioners do not identify them as such. Ex. 2010, ¶ 107. Petitioners' expert agreed in his deposition that Osanai does not teach that read leveling "*controls the timing*" of DQ or DQS signals entering the data buffer through lines L1 and L2, which Petitioners have identified as the claimed "*data paths*." *See* Ex. 2011, 98:21-99:1 ("Q. [W]ould you agree that Osanai does not teach that read leveling circuit 323 controls the timing of DQ entering the data buffer through lines L1 and L2? A. Yes."); *see id*, 99:8-12 (same for DQS signals). Thus, even if Petitioners could be credited with making this argument—and they cannot—it fails.

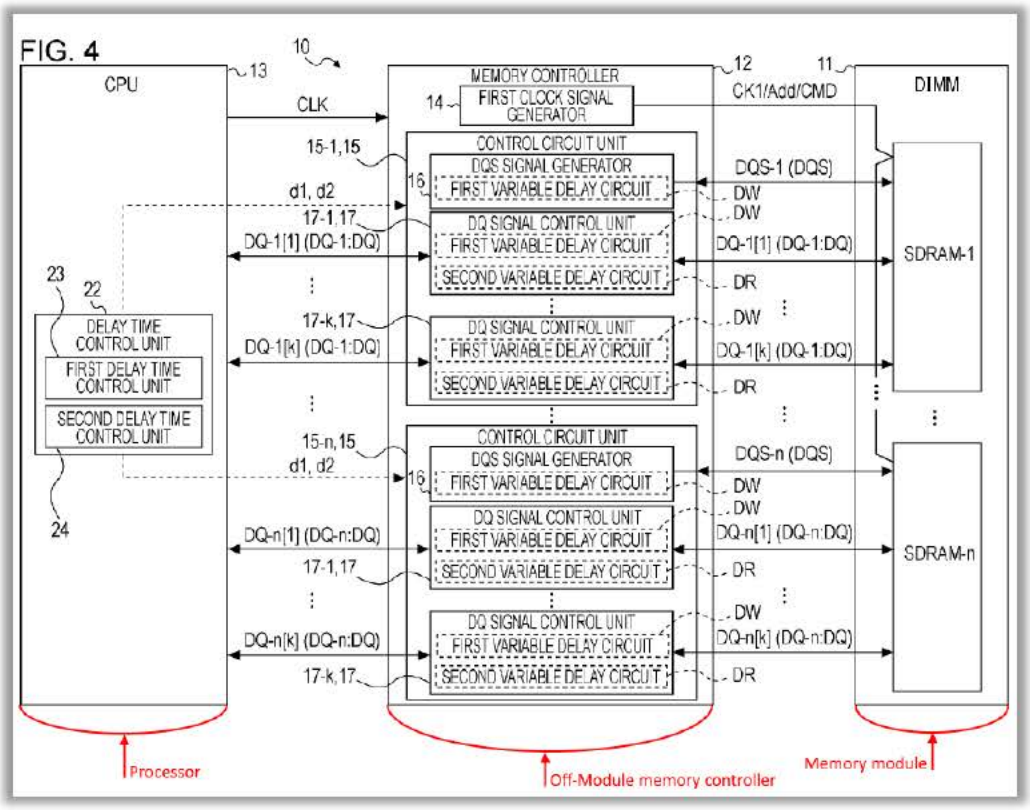
2. A POSITA would not have combined Osanai and Tokuhiro to arrive at the '035 claims (all claims).

Fundamentally, a POSITA would not have looked to Tokuhiro—which teaches improvements to an off-module memory controller—to improve the functionality of Osanai's on-module components. And even if a POSITA had considered Tokuhiro, both Osanai and Tokuhiro disclose known DDR3 write-leveling procedures, which would not have motivated a POSITA to improve Osanai in view of Tokuhiro. Moreover, Tokuhiro teaches a solution to a problem that does

not exist in Osanai—namely, an improved procedure for setting the delay through a set of variable delay lines that do not exist in Osanai. Petitioners' insistence that a POSITA would have incorporated Tokuhiro's leveling technique into Osanai's data register buffers requires impermissible hindsight and should be rejected.

a. A POSITA would not have looked to Tokuhiro's memory controller improvements to improve Osanai's buffer leveling circuitries.

As a threshold issue, a POSITA would not have looked to Tokuhiro to improve Osanai's memory module. Tokuhiro teaches improvements to an off-module memory controller—specifically how the CPU controls Tokuhiro's novel memory controller to eliminate the need for a separate read leveling step. Ex. 1006, 15:3-15, 16:19-22, 16: 29-35; Ex. 2010, ¶ 112. Dr. Alpert agreed. Ex. 2011, 100:9-16.



Ex. 1006, Fig. 4 (annotated); Ex. 2010, ¶ 112.

In contrast, Osanai's data register buffer 300 and command/address/control register buffer 400 are located on-module, distinct from Tokuhiro's off-module memory controller and processor. Ex. 1005, Fig. 1; Ex. 2010, ¶ 114. Petitioners assert that it would have been obvious to use Tokuhiro's technique in Osanai's buffer leveling circuitry because they are both directed to memory modules. Pet., 38-39. But, in fact, Tokuhiro does not teach improvements to the memory modules, themselves, but to the off-module controller. Ex. 2010, ¶ 115; *see also* Ex. 2011, 76:22-77:4, 90:6-17, 91:5-17. Petitioners argue in the alternative that both references are reasonably pertinent to the problem described by the '035 Patent—the

insufficiency of read and write leveling techniques. Pet., 38-39. However, Tokuhiro does not disparage JEDEC-specified write leveling, and does not mention or employ read leveling at all. Ex. 1006, 2:10-23, 2:46-49; Ex. 2010, ¶ 117.

In contrast, Osanai teaches improvements to the components of the memory module itself. Ex. 1005, Fig. 1, [0020], [0030-31], [0050-56]; Ex. 2010, ¶ 119. Osanai's inventive circuits and steps all occur **on** the memory module 100. Ex. 2010, ¶ 119. The data register buffer 300 and the command/address/control register buffer 400 are both located on the module. Ex. 1005, Fig. 1, Fig. 3, [0020], [0050-52]; Ex. 2010, ¶ 119. The read and write leveling circuits in Osanai's data register buffer 300 are autonomous and do not rely on the intervention of the CPU. Ex. 1005, [0096]; Ex. 2010, ¶ 119.

b. Tokuhiro is directed to solving a problem that does not exist in Osanai.

Moreover, Tokuhiro is fundamentally solving a problem that does not exist in Osanai. Specifically, Osanai teaches read leveling, the purpose of which is to set the timing for the input buffers INB. Ex. 1006, [0157]; Ex. 2010, ¶ 120. Tokuhiro does not mention—much less teach—read leveling. *See* Ex. 2010, ¶ 120. Both Tokuhiro and Osanai describe write leveling as a mechanism for adjusting write data and strobe timing so that write data arrives at the appropriate time. Ex. 1005, [0149-51]; Ex. 1006, 2:10-23, 2:46-49; Ex. 2010, ¶ 120. But unlike Osanai, Tokuhiro centers on techniques for determining the delay for read data passing through variable delay

circuits DR1 and DR2 by inferring the proper delay from the results of the previously performed write leveling. Ex. 1007, Abstract; Ex. 2010, ¶ 120. These variable delay circuits DR1 and DR2—which are the focus of Tokuhiro's invention—do not exist in Osanai. Ex. 1005, Fig. 5, [0090], [0093]; Ex. 2010, ¶ 121. Instead of Tokuhiro's flip flops FF5, FF6, FF7, and FF8 and variable delay circuits DR1 and DR2, Osanai discloses FIFO (Read) Circuit 302. Ex. 1005, Fig. 5, [0090], [0097]; Ex. 2010, ¶ 121.

Osanai does not need to determine the time Dt2 (from the time Dt1 or any other source) for the purposed of controlling the variable delay through DR1 and DR2 (via signal d2) because these variable delay circuits do not exist in Osanai. Ex. 1006, 15:3-15, 16:19-22, 16:29-35; Ex. 2010, ¶ 121. Thus, Tokuhiro's inventive aspect is simply not applicable to Osanai's structure and functionality. Ex. 2010, ¶ 122. A POSITA would not have been motivated to look to the teachings of Tokuhiro to modify Osanai. Ex. 2010, ¶ 122.

c. Petitioners have not shown how a POSITA would modify Osanai in view of Tokuhiro or that it would be feasible to do so.

Additionally, Petitioners have not shown *how* a POSITA would modify Osanai in view of Tokuhiro, or that it would be feasible to do so, even assuming one would have been motivated to modify Osanai in view of Tokuhiro. Any attempt to apply the teachings of Tokuhiro to Osanai's system would require substantial

changes to Osanai's hardware—which are not contemplated, explained, or justified by Petitioners—without benefit and substantial drawbacks. Ex. 2010, ¶ 123.

As one example, Osanai discloses read leveling to determine when to turn on the buffer chip input buffers INB to properly capture the read data from the memory devices. Ex. 1003, [0157]; Ex. 2010, ¶ 124. Tokuhiro derives from the write leveling procedure the amount of time that data needs to be delayed inside the memory controller so that it can be properly sent on to the CPU. Ex. 1006, 10:63-11:15; Ex. 2010, ¶ 124. Osanai's time to turn on input buffer INB and Tokuhuro's delay time are distinct, and the latter is not applicable anywhere within any of Osanai's embodiments. Thus, a POSITA could not have applied Tokuhiro's teachings to improve the determining of Osanai's INB buffer device enable time. Ex. 2010, ¶ 124.

As another example, Osanai's FIFO (Read) 302 aligns read data between when it arrives at 341 and 342 and when it is transmitted to the memory controller 340. Ex. 1005, [0093], [0097], [0135]; Ex. 2010, ¶ 125. Tokuhiro functions entirely differently: instead of including a FIFO in the read path as in Osanai, Tokuhiro includes DR1 and DR2, which ensure that read data arrives at FF6 and FF8, regardless of the phase relationship between the data arriving at the memory controller from the memory and when data has to go out to the CPU. Ex. 1006, 15:16-32, 15:62-16:28; Ex. 2010, ¶ 125. This function does not exist in Osanai,

which, instead, includes the FIFO (READ) 302. Ex. 1005, [0136]; Ex. 2010, ¶ 125. Further, the need for Osanai's read leveling—when to turn on the input buffers INB—does not exist in Tokuhiro because Tokuhiro's input buffers do not have a control input the way Osanai's input buffers do. *See* Ex. 1006, Fig. 9; Ex. 2010, ¶ 125. Thus, Tokuhiro teaches away from Petitioners' proposed modification. *See In re ICON Health & Fitness, Inc.*, 496 F.3d 1374, 1382 (Fed. Cir. 2007) ("[A] reference teaches away from a combination when using it in that combination would produce an inoperative result.").

Thus, Osanai's read leveling and Tokuhiro's adjustment of DR1 and DR2 based on write leveling results serve entirely different purposes, and their implementations are not substitutable. Ex. 2010, ¶ 126. Including the latter in Osanai's module would not achieve the desired results because it would not facilitate removing the read leveling circuit of Osanai or the eliminate the need for the read leveling operation to know when to turn on the input buffers INB—an important aspect of Osanai that Petitioners and Tokuhiro both ignore. Ex. 2010, ¶ 126. One cannot "stitch together an obviousness finding from discrete portions of prior art references without considering the references as a whole." *In re Enhanced Security Research, LLC*, 739 F.3d 1347, 1355 (Fed. Cir. 2014).

Petitioners do not attempt to reconcile these inherent inconsistencies. For example, the supporting paragraphs in Dr. Alpert's declaration say nothing about the

structure of the combination, how it would work, or what circuitry should be removed from Osanai or altered to accommodate Tokuhiro's teachings. Ex. 1003, ¶¶ 124-29; *see Roxane Labs., Inc. v. Novartis AG*, IPR2016-01461, Paper 9, 10 (P.T.A.B. Feb. 13, 2017) ("As the Board has stated repeatedly, conclusory expert testimony is entitled to little or no weight."); *see also Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) (stating that the Board has discretion to accord appropriate weight to broad conclusory statements from expert witnesses); *Rohm & Haas Co. v. Brotech Corp.*, 127 F.3d 1089, 1092 (Fed. Cir. 1997) (nothing requires a factfinder to credit the inadequately explained testimony of an expert). Instead, "[t]hroughout its discussion of rationales for combining the references, Petitioner[s] provide[] conclusory statements regarding what a person of ordinary skill 'would have understood,' citing the Alpert Declaration which merely mirrors the Petition with largely the same conclusory statements." *Microchip Tech. Inc. v. Hd Silicon Sols. LLC*, IPR2021-01420, Paper 13, 10 (P.T.A.B. May 12, 2022) (denying institution). That deficiency is dispositive.

d. Petitioners' proffered motivations are inapposite.

Instead of addressing the inherent inconsistencies between Osanai and Tokuhiro, Petitioners argue instead that it would have been obvious to use Tokuhiro's technique in Osanai's data register buffer leveling circuitries because doing so would (1) purportedly reduce the number of steps needed to determine the

read delay by basing that determination on timing information determined during write leveling; (2) reduce power consumption and circuit area, which Petitioners argue would reduce costs by increasing manufacturing yield; and (3) improve signal fidelity, decrease timing skew among components, and/or lower the load perceived by the memory controller. Pet., 38-41. But Petitioners proffered motivations are unavailing.

First, Petitioners are wrong that incorporating Tokuhiro's write leveling technique into Osanai's module would reduce the number of steps to determine the read delay. This assertion is wholly unsupported in the Petition. Pet., 39. As a primary matter, no comparable read delay is found or set in Tokuhiro. Ex. 2010, ¶ 130. Even Dr. Alpert does not explain how incorporating Tokuhiro's technique would provide the "same efficiency" to Osanai's memory module, or whether/how a product reflecting the combination would actually achieve that goal. *See* Ex. 1003, ¶ 126. He merely posits that it would "not be beyond the skill of an ordinary artisan." *Id.* This is insufficient to sustain Petitioners' claim of obviousness and does not demonstrate that such a combination would be operable for its intended purpose. *See Roxane Labs.,* IPR2016-01461, Paper 9, 10 ("As the Board has stated repeatedly, conclusory expert testimony is entitled to little or no weight.")

Second, Petitioners are wrong that incorporating Tokuhiro's write leveling technique into Osanai's module would reduce power consumption and circuit area,

or result in reduced costs by increasing manufacturing yield. Here, Petitioners focus on Tokuhiro's second embodiment, which uses a novel delay circuitry in Tokuhiro's memory controller that sets read and write path delays with one setting. Ex. 1006, 24:26–29. Petitioners posit that use of this circuitry would purportedly yield the recited efficiency when implemented on Osanai's memory module "without increasing the power consumption and the area." Pet., 40 (citing Ex. 1006, 24:26-29). But such circuit is not found in Osanai, and Petitioners do not suggest where in Figure 5 or elsewhere it could be incorporated or beneficially utilized. *See* Ex. 2010, ¶ 131. In fact, because Tokuhiro's DR1 and DR2 variable delay circuits have no analog in Osanai, adding an additional variable delay circuit would likely *increase* power and area. Ex. 2010, ¶ 131. In any event, Petitioners have not shown how the stated efficiency would materialize without increasing power or area in Osanai's circuitry. *See*, *e.g.*, *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998) ("Determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.").

Further, making a change **without increasing** power consumption/circuit area (as stated in Tokuhiro), is not equivalent to **reducing** power consumption/circuit area—Tokuhiro simply says that implementing its solution will not increase those things; it does not say it will decrease them as Petitioners claim. Ex. 2010, ¶ 132;

see also Ex. 2011, 137:4-14 ("Q. You would agree that there's a distinction between not increasing power consumption and area and decreasing power consumption and area, correct? A. Yes. There would certainly be a mathematical distinction.").

Lastly, Petitioners have not shown that incorporating Tokuhiro's use of the result of write leveling to determine an internal delay on the read path of Osanai's buffer would improve signal fidelity, decrease timing skew among components, or lower the load perceived by the memory controller. Again, Dr. Alpert provides no basis for or analysis of his conclusory opinion that it would, and the Board can therefore afford his testimony little or no weight. *Ex Parte Brian Huskinson, Michael Marshak, Michael J. Aziz, Roy G. Gordon, Theodore A. Bentley, Alan Aspuru-Guzik, Suleyman Er, & Changwon Suh*, No. APPEAL 2020-005269, 2021 WL 6194743, at *3 (P.T.A.B. Dec. 29, 2021); *Am. Acad. of Sci. Tech. Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations.") (citations omitted).

3. Petitioners fail to provide evidence that any reference renders obvious Claims 12 and 13.

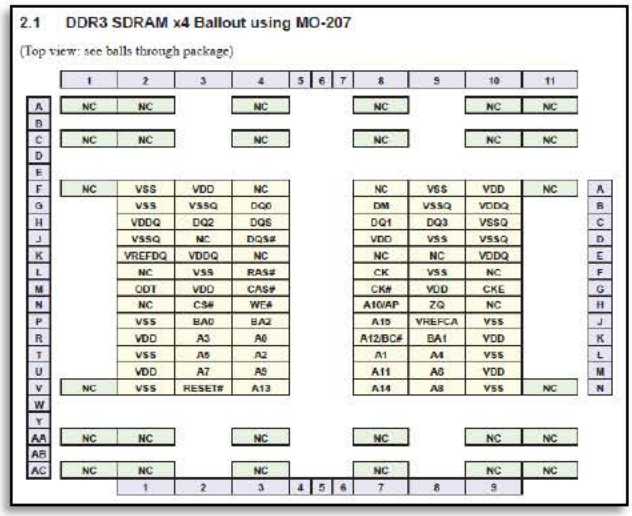
Claim 12 depends from Claim 1, and further requires "*wherein each of the plurality of buffer circuits has a data width of 1 byte, and wherein each of the memory devices has a data width of 4 bits*." Ex. 1001, cl. 12.

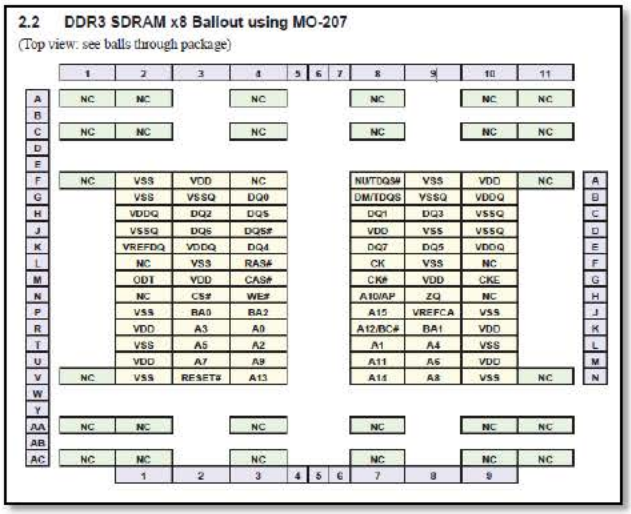
Petitioners' arguments for Claim 12 fail for the reasons that Claim 1 fails, as discussed above. *See supra*, Sections V.A.1-V.B.2. Additionally, Petitioners concede that Osanai does not teach a memory device with a data width of 4 bits. Pet., 44 ("each of Osanai's memory devices also has a data width of eight bits"). Nevertheless, Petitioners argue that a POSITA would have been motivated to modify Osanai's memory devices to use four bits instead of eight bits. *Id.*, 45. Each of Petitioners' arguments in support of this contention fails.

First, Petitioners assert that "different data widths were envisioned by Osanai," pointing to Paragraph [0196] of Osanai, which states that "memory chips 200 allocated to a single data register buffer 300 is not limited to a particular number." *Id.* This language, however, is not a suggestion that a POSITA would use data widths other than 8 bits. Ex. 2010, ¶ 142. It relates instead to having more *ranks*, as made clear by the language Petitioners omit from their carefully excerpted quote: "That is, **the number of** memory chips 200 allocated to a single data register buffer 300 is not limited to a particular number **as long as it is equal to or larger than two**." Ex. 1005, [0196] (emphasis added); Ex. 2010, ¶ 142. Petitioners again resort to distorting the cited references, using impermissible hindsight to bridge the gaps in their proof. *See ATD Corp.*, 159 F.3d at 546 ("Determination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.").

Petitioners also assert that a POSITA would have used four bits to "comply with the commercial standardization of DDR3 SDRAMs, which specified 4 bits." Pet., 45. But the DDR3 standards specify myriad features that may or may not function well, be compatible with a given disclosure, or provide motivation to a POSITA. Ex. 2010, ¶ 143. This argument is unavailing.

Additionally, Petitioners' argument that a person would have been motivated to reduce packaging costs is belied by the very evidence they cite to. Pet., 45. Specifically, Petitioners cite page 3 of JESD79-3C, which is the portion of the DDR3 standard relating to "Package Pinout and Addressing," but do not explain why it supports their position. *See id.* (citing Ex. 1013, 3). On page 3 of the standard, however, the 4-bit and 8-bit devices are in the very same package, making clear that any purported reduction in packing costs would not actually be realized:





See Ex. 1013, 3-4 (showing the same package for DDR3 SDRAM x4 and DDR3 SDRAM x8); Ex. 2010, ¶ 144. Moreover, narrower devices are not inherently cheaper to manufacture. *See* Ex. 2010, ¶ 144.

Petitioners also argue, incorrectly, that using a data width of four bits would have been a "common design tradeoff." Pet., 45. But it is not inherently true that 4-bit modules have simpler routing than 8-bit modules. Ex. 2010, ¶ 145. Nor is it true that 4-bit modules necessarily have higher density or improve speed by having fewer devices connected to each data line. Ex. 2010, ¶ 145. Given that the packages and module dimensions for each as identified in the standard are the same, the number of die per package will also be the same. Ex. 2010, ¶ 145. The bits may be organized differently, but the number of bits that can be fit onto a module is the same in both cases. Ex. 2010, ¶ 145. Petitioners' cited portion of the DDR3 standard, again, does not support Petitioners' argument; the standard defines the same speed grades for the 4-bit and 8-bit SDRAMs. Ex. 2014, 128, 144-148; Ex. 2013, 128, 147-51; *see* Ex. 2010, ¶ 145.

Lastly, Petitioners argue that modifying Osanai's memory module to implement a data width of 4 bits "would simply arrange old elements with each performing the same function it had been known to perform and yields no more than one would expect from such an arrangement, and would therefore have been obvious." Pet., 45. Petitioners rely on Dr. Alpert's testimony, which merely parrots

the same language with no further explanation or analysis. *Id.* (citing Ex. 1003, ¶ 140). But Petitioners' (unsupported) argument is incorrect because design complications resulting from splitting bus widths at the data register buffers would dissuade a POSITA from making the proposed modification, especially in the absence of a benefit from using 4-bit devices with 8-bit data register buffers. Ex. 2010, ¶ 146. As a result, Petitioners have not shown that a POSITA would have been motivated to modify Osanai's memory devices to use four bits instead of eight bits, and Petitioners' arguments regarding Claim 12 fail. Ex. 2010, ¶ 147.

Claim 13 depends from Claim 12 (and further from claim 1). Petitioners' arguments relating to Claim 13 fail for the same reasons as Claims 1 and 12, described above and *supra* in Sections V.A.1-V.B.3. Ex. 2010, ¶ 148.

4. Petitioners fail to provide evidence that any reference discloses or renders obvious Claims 2, 6, 10, 21, and 22.

Petitioners' arguments relating to Claims 2, 6, 10, 21, and 22 fail for the same reasons as Claim 1, described *supra* in Sections V.A.1-V.B.2. Ex. 2010, ¶ 149.

C. Ground 2: Petitioners' proposed combination of Takefman and Tokuhiro does not disclose all limitations of the challenged claims.

Petitioners have not even *alleged* that Takefman satisfies each claim limitation. Nor could they, as the architecture disclosed in Takefman is fundamentally different than the '035 Patent. In numerous instances, Petitioners appear to concede that Takefman does not disclose the limitations as claimed and

instead rely on the knowledge of a POSITA—supported by expert opinion that is conclusory and smacks of hindsight—to argue it would have been obvious to make modifications. Petitioners simply have not carried their burden to show that the proposed combination of Takefman and Tokuhiro discloses or renders obvious each claim limitation.

1. Petitioners fail to provide evidence that Takefman discloses or suggests a "*module control device*" (all claims).

The claims require "*a module control device mounted on the module board and configured to receive memory command signals for a first memory operation from the memory controller via the set of control/address signal lines and to output module command signals and module control signals in response to the memory command signals*." Ex. 1001, cl. 1. The claims further specify that the "*module control device*" sends "*module command signals*" to the claimed memory devices and "*module control signals*" to the claimed buffer circuits. *Id.* Thus, any "*module control device*" identified by Petitioners must be shown to be configured to (1) receive "*memory command signals*" from the memory controller via control/address signal lines, (2) output "*module command signals*" to memory devices, and (3) output "*module control signals*" to buffer circuits. *Id.*

Petitioners allege that Takefman's Rush 301 is the claimed "*module control device*." Pet., 53. But Petitioners wholly fail to allege, much less show, where Takefman discloses that Rush 301 outputs any claimed "*module command signals*"

to any memory device or any claimed "*module control signals*" to any claimed buffer. In fact, Petitioners' analysis for these particular claim limitations is **one sentence total**; Petitioners merely—and conclusorily—state that that "[a POSITA] would also have understood that Rush 301 outputs "*module command*" and "*control signals*" for the first memory operation (a read operation)," citing to Dr. Alpert's declaration *Id.*, 55 (citing Ex. 1003, ¶ 164) (emphasis in original). But Dr. Alpert merely repeats the same conclusory language that is in the Petition, while providing no additional explanation, analysis, or support. Ex. 1003, ¶ 164.

Indeed, Petitioners have not attempted to show that Rush 301 communicates at all with the DRAM 302 devices, which Petitioners allege are the claimed "*memory devices*." Takefman does not, in fact, teach that Rush 301 communicates directly with the DRAM 302 devices which, instead, communicate directly with the Bolt 303 devices, as shown in Petitioners' own annotated image:

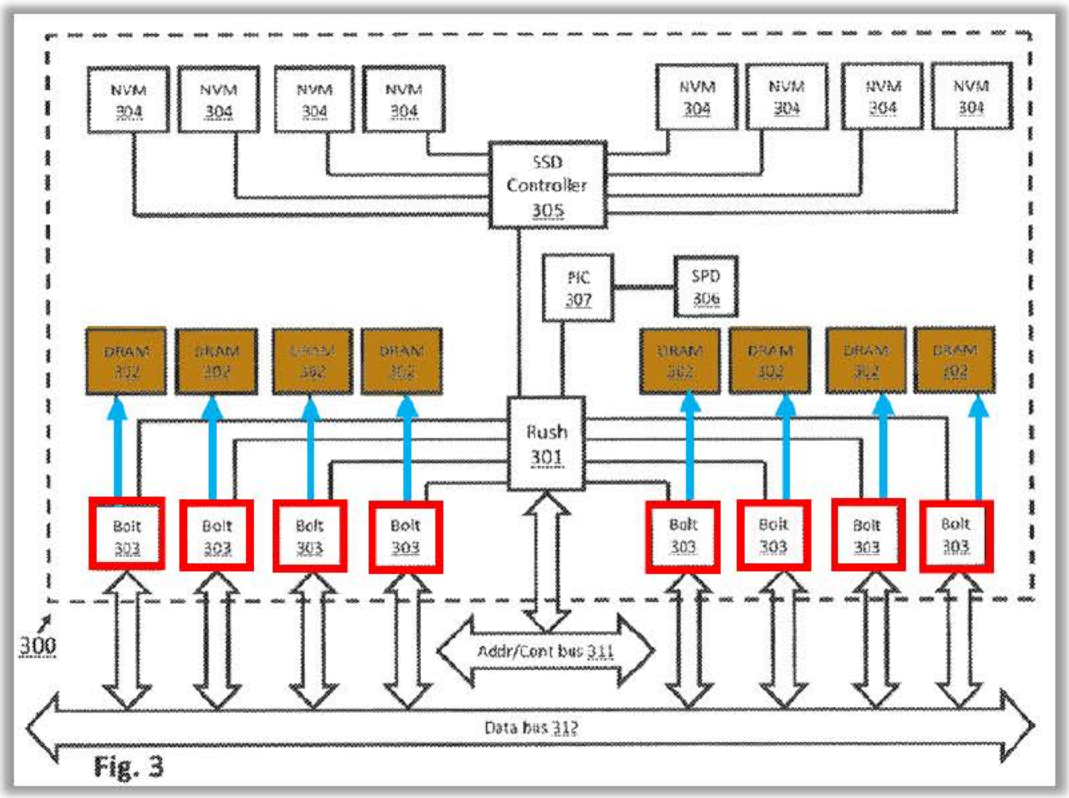


Fig. 3

Pet., 59; *see also* Ex. 2010, ¶ 158. In his deposition, Dr. Alpert conceded that there is no direct connection between Rush 301 and the DRAM devices 302 and that Takefman does not disclose any signals sent from Rush 301 to the DRAM devices 302. *See* Ex. 2011, 107:11-15, 108:16-18. This constitutes a wholesale failure of proof; Petitioners have not shown that Takefman discloses or renders obvious this claim element (and do not contend that Tokuhiro does, either).

Petitioners' groundless, gratuitous, unsupported statements cannot carry their burden to invalidate the '035 Patent. *See A123 Sys., LLC v. Long Hua Tech. Co., LTD.*, IPR2021-00894, Paper 12, 18 (P.T.A.B. Oct. 18, 2021) (denying institution where Petitioner failed to show where in the cited reference each claim element was

disclosed). Petitioners' arguments are therefore facially deficient as to Takefman, and the remainder of Grounds 2 and 3 fail as a result.

2. Petitioners fail to provide evidence that Takefman discloses or suggests "*memory devices*" that are "*configured to perform the first memory operation in response to the module command signal*" (all claims).

The claims require "*memory devices mounted on the module board and configured to perform the first memory operation in response to the module command signals, the memory devices including a plurality of sets of memory devices corresponding to respective sets of the plurality of sets of data/strobe signal lines*." For this claim limitation, Petitioners point to Takefman's DRAM 302 as the claimed "*memory devices*." Pet., 55-56. But, again, Petitioners do not attempt to show that DRAM 302 performs any "*memory operation*" "*in response to the module command signals*" as required by the claims—because Petitioners have not identified any "*module command signals*" at all. *See supra* Section V.C.1. Instead, Petitioners state merely that a "POSITA would have recognized that DRAM 302 receives '*module command signals*' from Rush 301 that instruct the DRAM to perform certain operations, such as a write operation (a "*first memory operation*")," citing to another conclusory sentence from Dr. Alpert's declaration that does not include any further explanation, analysis, or support for his opinion or Petitioners' specious assertions. *Id.* (citing Ex. 1003, ¶ 168) (emphasis in original).

Because Petitioners have not identified where Takefman discloses "*module command signals*" sent from a "*module control device*" to the claimed "*memory devices*," Petitioners' proof for this claim element also fails. *See supra* Section V.C.1.

3. Petitioners fail to provide evidence that Takefman discloses or suggests the claimed "*logic configured to respond to the module control signals by enabling the data paths*" (all claims).

The claims also require the claimed "*logic*" to be "*configured to respond to the module control signals by enabling the data paths*." Ex. 1001, cl. 1. For this claim element, Petitioners point to Takefman's disclosure of "per-lane compensation circuits that . . . provide programmable launch times and lane de-skew on receive." Pet., 61. Specifically, Petitioners state that a POSITA would have recognized that such circuits are "'*logic*' that enable data paths for control signals at appropriate launch times to ensure 'data arrives at the appropriate time.'" *Id.* (emphasis in original). But Petitioners do not allege anywhere in the Petition that such circuits are configured to respond to the claimed "*module control signals*" sent from the "*module control device*" to the "*buffer circuits*." Thus, as a preliminary matter, Petitioners have not shown that Takefman discloses the claimed "*logic*." *See* Ex. 2010, ¶ 169.

Moreover, Petitioners rely on functionality not even present in what Petitioners assert are the claimed "*buffers*." Petitioners point to "per-lane delay compensation circuits" in **Rush 301**, which Petitioners assert is the "*module control*

device." Pet., 61 ("Takefman discloses that Rush 301 includes 'per-lane delay compensation circuits that . . . provide programmable launch times and lane de-skew on receive.'"); Ex. 2010, ¶ 170. But the claims require the claimed "*logic*" to be included in the claimed "*buffer circuits*," not the "*module control device*." Ex. 1001, cl. 1 ("*each respective buffer circuit including . . . logic configured to respond to the module control signals by enabling the data paths*"). And so, again, Petitioners have not shown that Takefman discloses the claimed "*logic*." *See* Ex. 2010, ¶ 170.

Petitioners appear to concede that such circuits do not actually satisfy the claim language, because Petitioners also state that, "[t]o the extent that Netlist argues that Takefman's buffers do not include the claimed '*logic*,' Takefman in view of the knowledge of a skill [sic] artisan renders this interpretation obvious." Pet., 62. Petitioners argue that a POSITA would have been motivated to modify the teachings of Takefman "to include logic that both performs compensation adjustments and enables data paths" based on Dr. Alpert's declaration. *Id.* But again, Petitioners and Dr. Alpert wholly fail to even allege that a POSITA would have modified Takefman to include "*logic*" that is "*configured to respond to the module control signals*" sent from the "*module control device.*" *See id.*; *see also* Ex. 1003, ¶ 185. And, as previously made clear, Petitioners have not even identified the claimed "*module control device*" in Takefman, *see supra* Section V.C.1, highlighting once again the significant distinction between Takefman and the architecture disclosed in the '035

Patent. Thus, even if a POSITA would have been motivated to modify Takefman as Petitioners contend, Takefman would still not satisfy the claim language. *See supra* Section V.C.1; *see* Ex. 2010, ¶ 171. Petitioners' proof for this claim element fails, compounding Petitioners lack of proof to support Ground 2.

4. Petitioners fail to provide evidence that Takefman, in view of Tokuhiro, discloses or suggests the claimed "*logic . . . further configured to obtain timing information . . . during a second memory operation*" and "*control timing of the respective data and strobe signals on the data paths in accordance with the timing information*" (all claims).

The claims also require the claimed "*logic*" to be further configured to "*obtain timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation and to control timing of the respective data and strobe signals on the data paths in accordance with the timing information*." Ex. 1001, cl. 1. Thus, Petitioners must show that the proposed combination of Takefman and Tokuhiro includes "*logic*" that is configured to (1) obtain timing information received during a second memory operation and (2) control timing of the data/strobe signals in accordance with that timing information. As described below, they have not.

Petitioners contend that "Takefman discloses the claimed '*logic*'. . .," but concede that Takefman, "does not expressly disclose that the timing information is obtained '*during a second memory operation prior to the first memory operation*'," relying instead on Tokuhiro as allegedly satisfying this limitation. *See* Pet., 63. As

previously made clear, however, Takefman does not disclose the claimed "*logic*," and it would not have been obvious for a POSITA to have modified Takefman's Bolt 303 devices in a way that satisfies the claims. *See supra* Section V.C.3; Ex. 2010, ¶¶ 155-60. Nor does Tokuhiro teach "*obtaining timing information based on one or more signals received by the each respective buffer circuit during a second memory operation prior to the first memory operation*," for the reasons outlined above. *See supra* Section V.A.

But even beyond those deficiencies, Petitioners have failed—yet again—to even allege that either Takefman or Tokuhiro discloses **all** of the required claim limitations. Specifically, Petitioners have not identified where the proposed combination of Takefman and Tokuhiro discloses the claimed requirement that the buffer circuit's "*logic*" be "*further configured to . . . control timing of the respective data and strobe signals on the data paths in accordance with the timing information*." Ex. 1001, cl. 1. The only analysis Petitioners offer relating to how the combination allegedly "*control[s]*" the "*respective data and strobe signals on the data paths*" in accordance with the "*timing information*" purportedly obtained during Tokuhiro's write leveling procedure relates to the "per-lane compensation circuit" in Takefman's Rush 301. *See* Pet., 63. Specifically, Petitioners contend that a POSITA would have recognized that "Takefman's launch times adjustment and lane de-skew is '*control[ing] timing of the respective data and strobe signals on the data*

paths in accordance with the timing information.'" *Id.*, 64 (emphasis in original). But in so arguing, Petitioners again employ imprecise language to circumvent the claims' express requirements, and Petitioners' assertions, on their face, are insufficient.

First, Petitioners again point to functionality located in Takefman's Rush 301—the purported "*module control device*"—to satisfy functionality that the claims make clear must be within the "*buffer circuits*." *See* Ex. 1001, cl. 1; Ex. 2010, ¶ 180. To the extent that Petitioners intended to argue that a POSITA would know how to incorporate such functionality into Takefman's Bolt 303 devices, Petitioners do not actually make that argument and cannot be credited with it. *See Sirona Dental Sys. v. Institut Straumann AG*, 892 F.3d 1349, 1356 (Fed. Cir. 2018) (it would "not be proper for the Board to deviate from the grounds in the petition and raise its own obviousness theory.").

Further, Petitioners' analysis offered in support of their assertion that Takefman teaches such functionality is conclusory at best. Dr. Alpert does not explain how the "per-lane compensation circuit" that purportedly "provide[s] programmable launch times and lane de-skew on receive" satisfies the claims' requirement that the "*buffer circuit*" include "*logic*" configured to "*control timing*" of (1) "*respective data and strobe signals*" (2) *"on the data paths*" (3) "*in accordance with the timing information*." Ex. 1003, ¶¶ 184-88. Petitioners' bald

assertion that a POSITA could have "modified Bolt devices 303 to include logic that both performs compensation adjustments and enables data paths" is also insufficient to satisfy the "*control timing*" requirement because Petitioners do not demonstrate that such logic would "*control timing*" of any "*data/strobe signals*" on what Petitioners contend is the claimed "*data path*" (as opposed to some generic data path).[17]

For these reasons, Petitioners have not carried their burden to establish that the proposed combination of Takefman and Tokuhiro disclose each of the claimed limitations.

5. A POSITA would not have combined Takefman and Tokuhiro to arrive at the '035 claims (all claims).

Ground 2 requires a complete redesign of Takefman's memory module, which is wholly incompatible with Tokuhiro's memory controller. Neither Takefman nor Tokuhiro provide motivation for a POSITA to do so, thus Ground 2 fails.

a. A POSITA would not have looked to Tokuhiro's memory controller improvements to improve Takefman's memory module.

As with Osanai, a POSITA would not have looked to Tokuhiro's off-module memory controller to improve Takefman's completely disparate architecture. As a

[17] As claimed, the "data path" must be "for transmitting respective data and strobe signals associated with the first memory operation." Ex. 1001, cl. 1.

threshold matter, because Takefman does not disclose fly-by signal routing topology for any control or address lines as Tokuhiro does, Takefman does not present a need to obtain timing information during a memory operation, even if Tokuhiro did teach that (which, for the reasons described above, it does not). Ex. 1006, 2:10-12, 2:46-49, 5:23-41; Ex. 2010, ¶ 186; *see* Ex. 2011, 103:21-104:4, 104:11-17 ("Q. Is it fair to say that you don't have an opinion one way or another, sitting here today, as to whether Takefman teaches the DDR3 fly-by topology? A. I would agree."). Specifically, in the absence of a fly-by distribution of clock and the topology of the DRAMs 302 and Bolt devices 303, clock and DQS would arrive simultaneously at the DRAMs, and therefore write leveling would be unnecessary. Ex. 2010, ¶ 186. As a result, there would simply be no benefit from adding Tokuhiro's compensation circuitry to Takefman's system, regardless of whether doing so would be within the skill of a POSITA. Ex. 2010, ¶ 188; *see Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed. Appx. 1019, 1027 (Fed. Cir. 2016) ("what one of skill in the art . . . 'could have' done to meet the limitation . . . is not sufficient").

Moreover, Takefman solved the problems posed by varying propagation delay via "launch time adjustments and lane de-skew," which Petitioners' expert concedes. Ex. 1007, 6:14-20; Ex. 2010, ¶ 189; Ex. 2011, 106:1-5. A POSITA would not have been motivated to incorporate Tokuhiro's solution taught into Takefman to solve the same problem in a different way. Ex. 2010, ¶ 189. In other words, there is no problem

in Takefman that would be addressed by adding Tokuhiro's write-leveling that is not already addressed by Takefman's own mechanisms. Ex. 2010, ¶ 189; *see Arris Int'l PLC v. Sony Corp.*, IPR2016-00828, Paper 10, 15-16 (P.T.A.B. Oct. 7, 2016) (rejecting petitioner's obviousness rationale that "fails to acknowledge that [the primary prior art reference] already provides a different solution to the problem identified by Petitioner"); *Front Row Techs. v. MLB Advanced Media, L.P.*, IPR2015-01932, Paper 7, 17 (P.T.A.B. Mar. 25, 2016).

Finally, Takefman's functionality on which Petitioners rely is not located in "*buffer circuits*" as required by the claims. Petitioners point primarily to functionality in Takefman's Rush 301, which Petitioners identify as the claimed "*module control device*." Pet., 53; *see* Ex. 2010, ¶ 190. Petitioners do not explain, however, why a POSITA would have been motivated to incorporate Tokuhiro's write-leveling functionality into Takefman's Bolt devices 303 (which already include retiming circuits), or how they would have done so. Ex. 2010, ¶ 190. Contrary to Petitioners' conclusory assertion, there is no indication that this combination would yield predictable or beneficial results. Ex. 2010, ¶ 190.

b. Petitioners' proffered motivations are inapposite.

Petitioners do not address any of the limitations discussed above and, instead, recycle their motivation arguments for Ground 2. For the reasons discussed *supra*, such arguments are unavailing. *See supra*, Section V.B.2.

6. Petitioners fail to provide evidence that any reference discloses or renders obvious Claims 2, 6, 12, 13, and 21.

Petitioners' arguments relating to Claims 2, 6, 12, 13, and 21 fail for the same reasons as Claim 1, described *supra* in Sections V.A., V.C.[18] Ex. 2010, ¶ 193

D. Ground 3: Petitioners' proposed combination of Osanai, Takefman, and Tokuhiro does not disclose all limitations of the challenged claims.

The entirety of Petitioners' analysis in support of Ground 3 spans less than a page and a half. Pet., 70-71. It is unclear from Petitioners' analysis what the proposed combination of Osanai, Takefman, and Tokuhiro even is, as Petitioners merely allege—with no support, evidence, or accompanying analysis—that "[a] POSITA would have been motivated to modify Takefman in the manner described in Ground 2 to include Osanai's teachings." *Id.*, 71. Petitioners do not describe **which** teachings from Osanai would be included in the proposed modification of Takefman's memory module, or why a POSITA would be motivated to modify Takefman in view of Osanai, specifically.[19] *See id.* Petitioners cannot be credited with arguments they did

[18] Petitioners have not asserted that claims 10-11, or 22 are rendered obvious over Takefman in view of Tokuhiro. Pet., 109-115.

[19] Petitioners point to their motivation arguments from Ground 1's combination of Osanai and Tokuhiro and Ground 2's combination of Takefman and Tokuhiro, but

not bother to make with any specificity. *See Universal Imaging Indus., LLC v. Lexmark Int'l, Inc.*, IPR2019-01381, Paper 7, 21 (P.T.A.B. Feb. 3, 2020) (citing *In re Magnum Tools Int'l, Ltd.*, 829 F.3d 1364, 1381 (Fed. Cir. 2016)) ("We will not, and cannot, piece together Petitioner's inconsistent and contradictory arguments into a cogent and coherent explanation that supports anticipation. Rather, we must evaluate the Petition's arguments as presented.").

But even if Petitioners had disclosed their proposed combination with sufficient specificity, Ground 3 fails for the same reasons that Ground 2 fails. Specifically, Petitioners have not demonstrated that Takefman discloses the claimed "*module control device*"; "*memory devices*" that are "*configured to perform the first memory operation in response to the module command signal*"; "*logic configured to respond to the module control signals by enabling the data paths*"; or "*logic . . . further configured to obtain timing information*." *See supra* Section V.C.1-V.C.4. Moreover, a POSITA would not have been motivated to combine either Osanai and Tokuhiro or Takefman and Tokuhiro for the reasons described herein. *See supra*

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those arguments plainly do not address why a POSITA would have been motivated to modify Takefman in view of Osanai. *See* Pet., 71.

Section V.C.5. Because none of the analysis proffered by Petitioners in support of Ground 3 cures these deficiencies, Ground 3 is also unavailing.[20]

VI. CONCLUSION

For the foregoing reasons, Patent Owner respectfully requests the Board confirm that the challenged claims of U.S. Patent No. 9,824,035 are patentable.

[20] Petitioners do not dedicate any analysis to the dependent claims for Ground 3. Thus, for the reasons articulated *supra* in Section V.D, Petitioners' proof for Claims 2, 6, 12, 13, and 21 fails. Petitioners have not asserted that Claims 10-11, or 22 are rendered obvious over Takefman in view of Tokuhiro, in further view of Osanai. Pet., 116.

Dated: October 11, 2022

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CERTIFICATE OF WORD COUNT

Under the provisions of 37 C.F.R. § 42.24(b)(2) and (d), the undersigned hereby certifies that the Microsoft Office word count for the foregoing Patent Owner's Response Under 37 C.F.R. § 42.120, excluding the table of contents, table of authorities, claim listing, certificate of word count, and certificate of service, totals 13,458 words, which is less than the 14,000 words allowed under 37 C.F.R. § 42.24(b)(2).

Dated: October 11, 2022

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CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e), I certify that I caused to be served on the counsel for Petitioners a true and correct copy of the foregoing Patent Owner's Response Under 37 C.F.R. § 42.120, by electronic means on October 11, 2022, by delivering a copy via electronic mail to the attorneys of record for the Petitioners as follows:

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